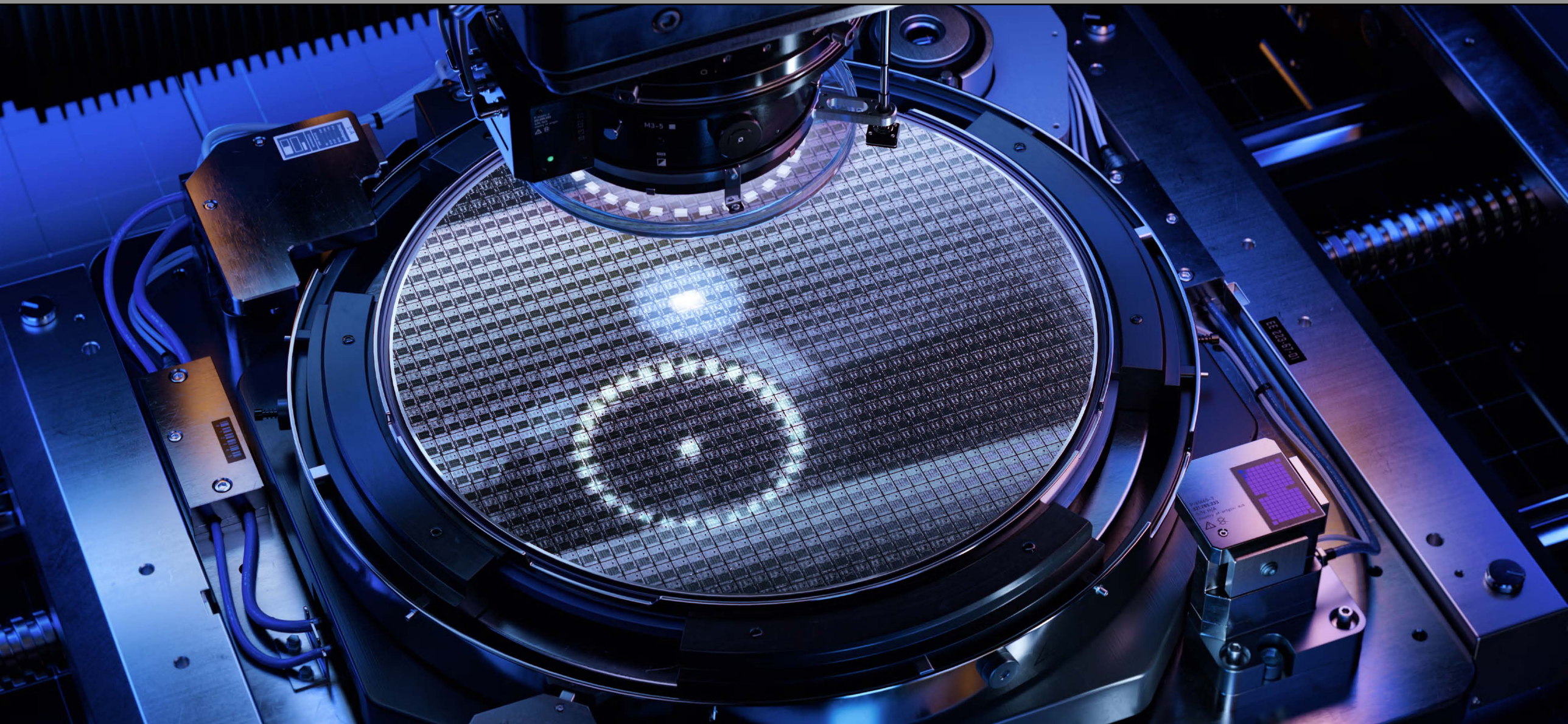
Layered Manufacturing

Thin Film Processes: MEMS and Microelectronics



Layered Manufacturing

Thin Film Processes: MEMS and Microelectronics

2.008 Coverage

Thin Film Processes

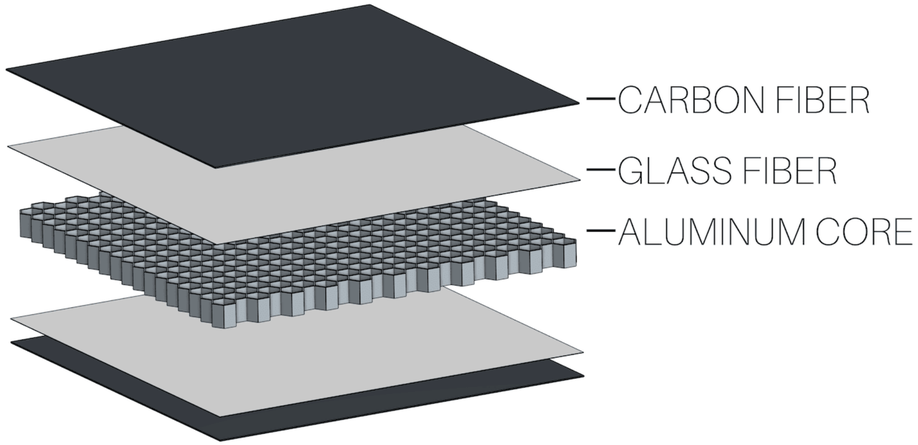
MEMS

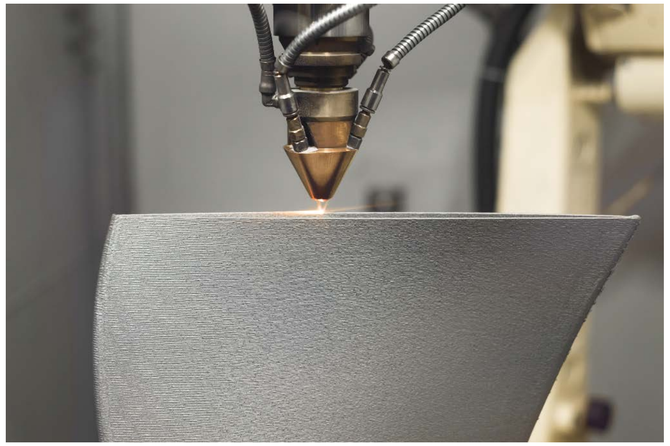
Microelectronics

Surface Coating

Layered Composites Manufacturing

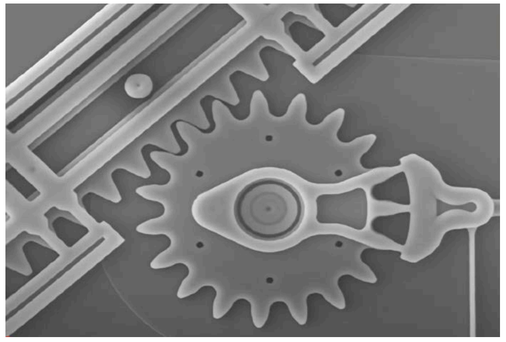
Additive Manufacturing



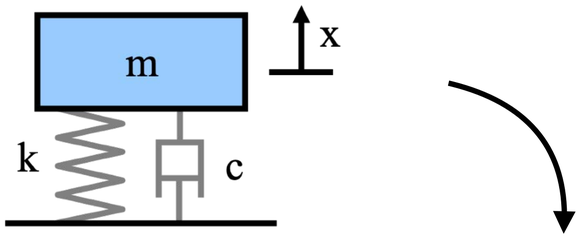


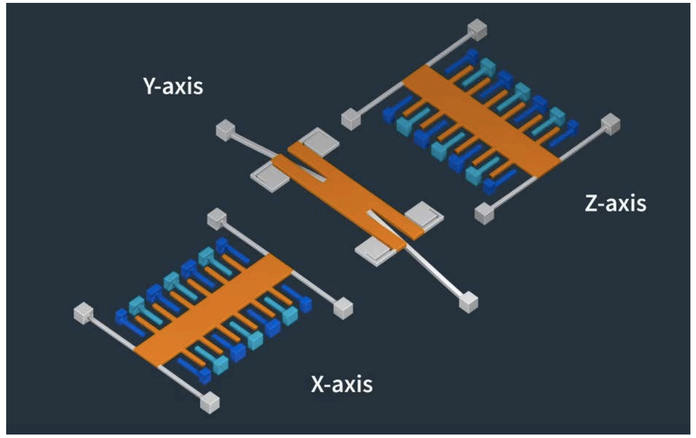
MEMS: Micro-electromechanical Systems

- μm scale: small but mighty
- integrated systems of sensing, actuation, communication, control, power and computing
- low **power**
- low **cost**
- rapidly developing field: chemical, bio, fluidic, optical, pharma



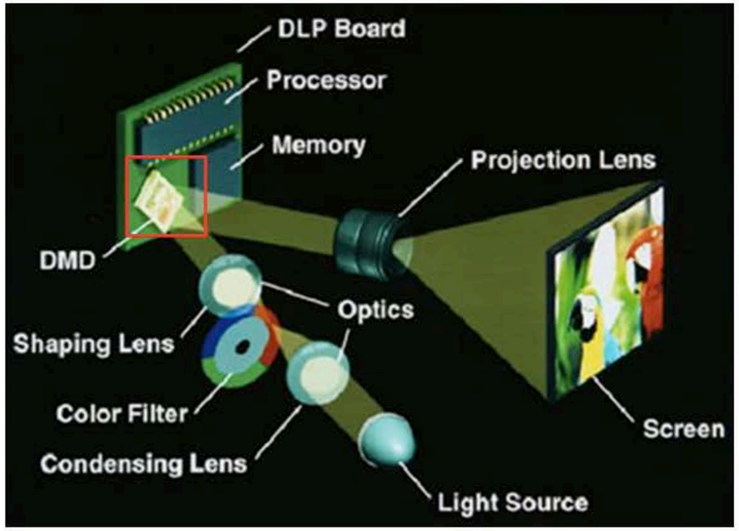
Accelerometers



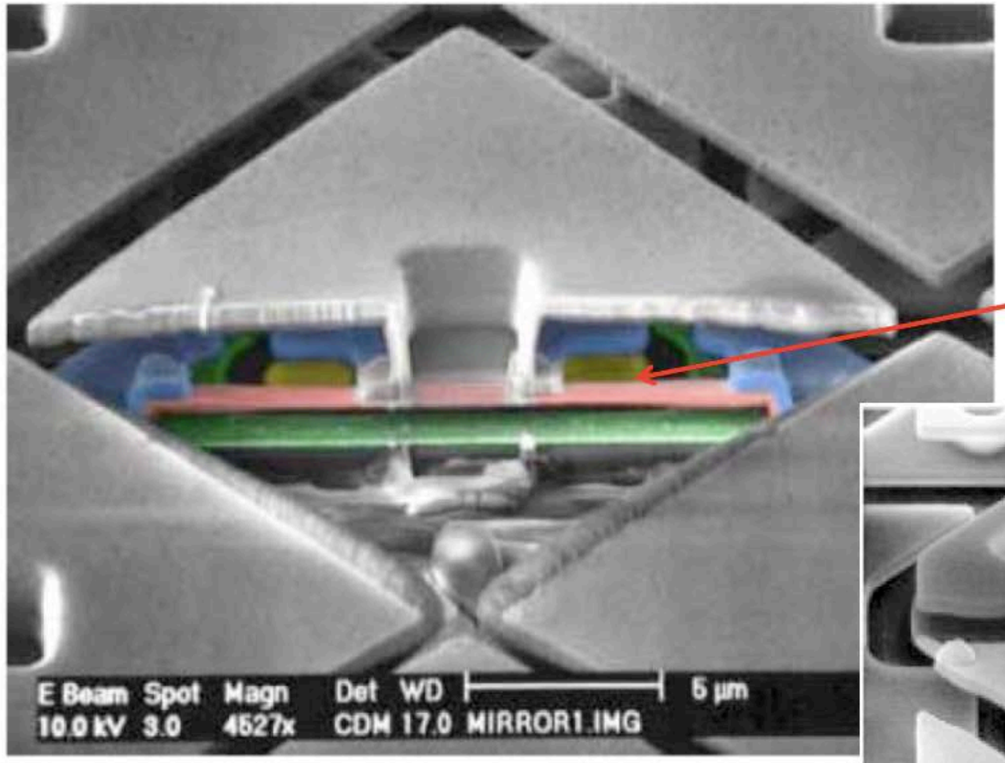


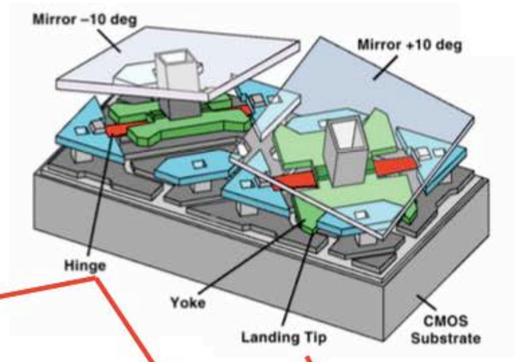
- airbags: low cost allows for democratization of technology

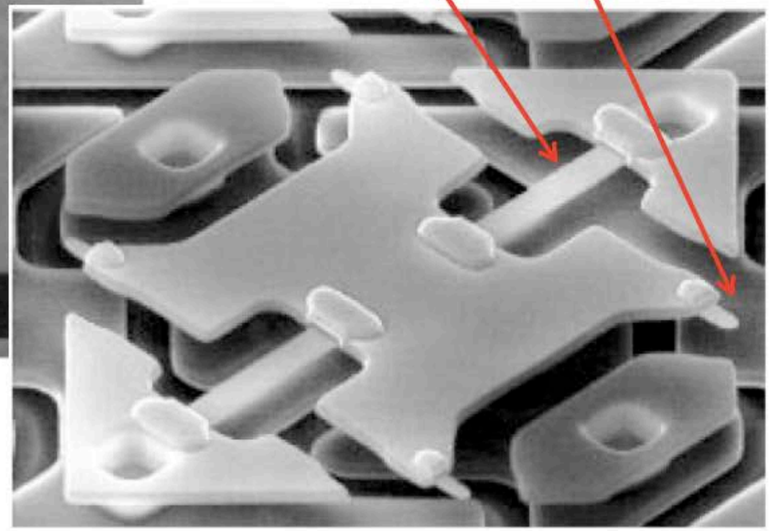
DMD (Digital Micromirror Device) for DLP (Digital Light Processing)



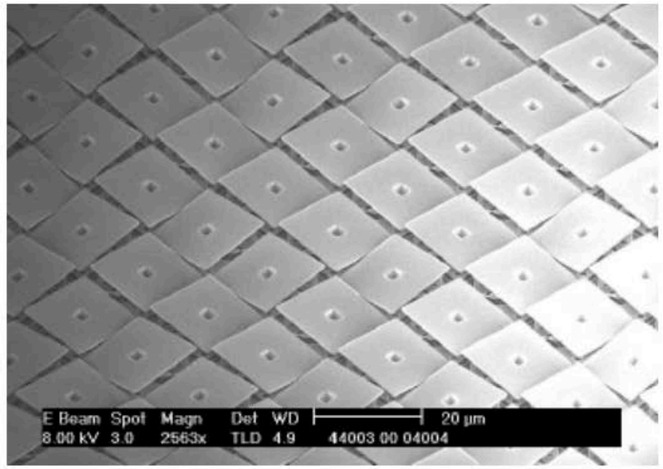
MEMS: Micro-electromechanical Systems







DMD (Digital Micromirror Device) for DLP (Digital Light Processing)



2000 x 1000 = 2 million mirrors!

each mirror 5 x 5 µm!

fatigue life: 10^{12} cycles!

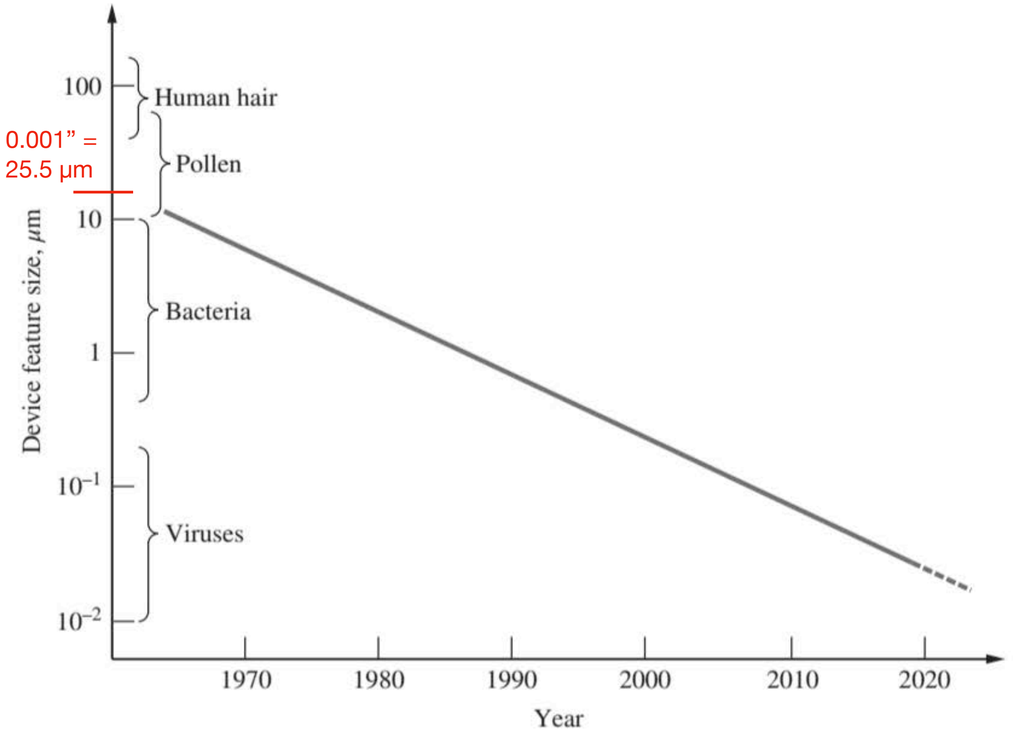
Micro-electronic Devices

0.03 vs 0.02 ¢/hour

increase in performance compared to “macro” technologies while decreasing cost

- what’s the downside?
- huge investment in technology and manufacturing processes to get economy of scale

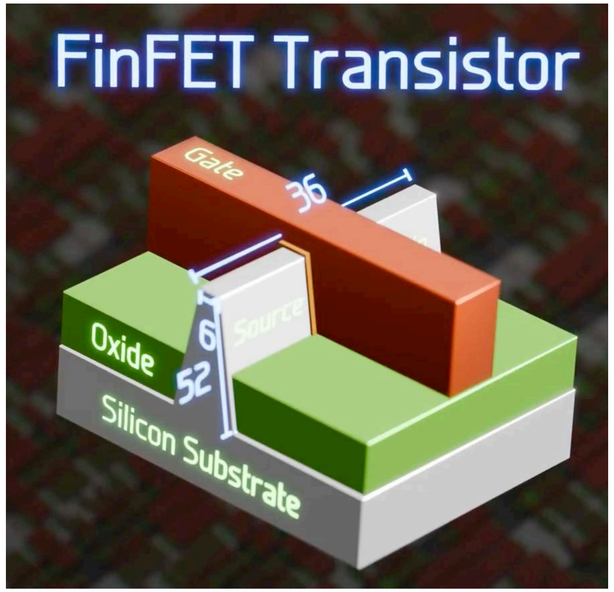
Manufacturing Across Scales



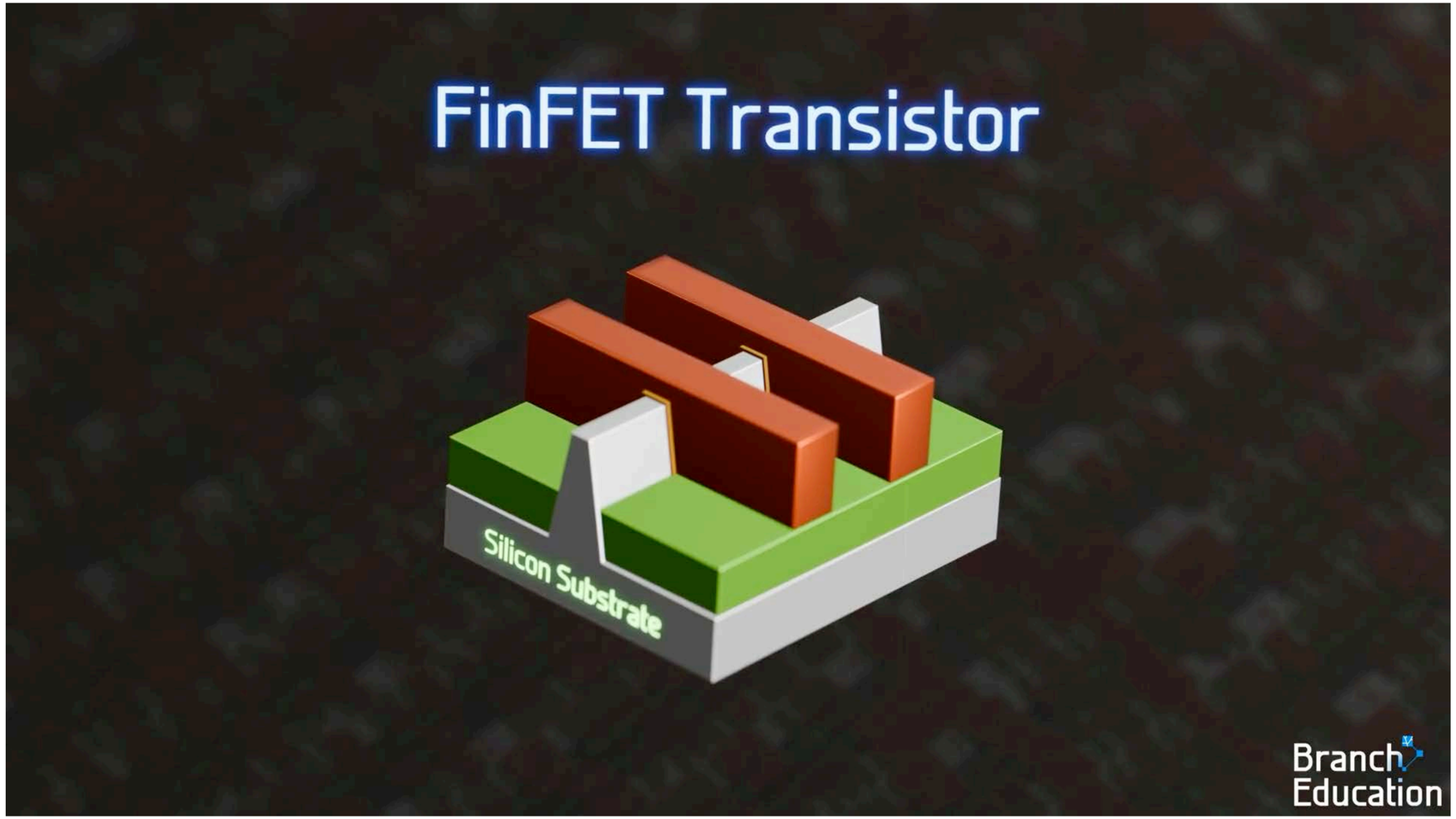
■ **Figure 33.4** Trend in device feature size in IC fabrication; also shown is the size of common airborne particles that can contaminate the processing environment. Minimum feature sizes for logic type ICs are projected to be about 5 nm in 2020 [25].

graphics and animations: Branch Education

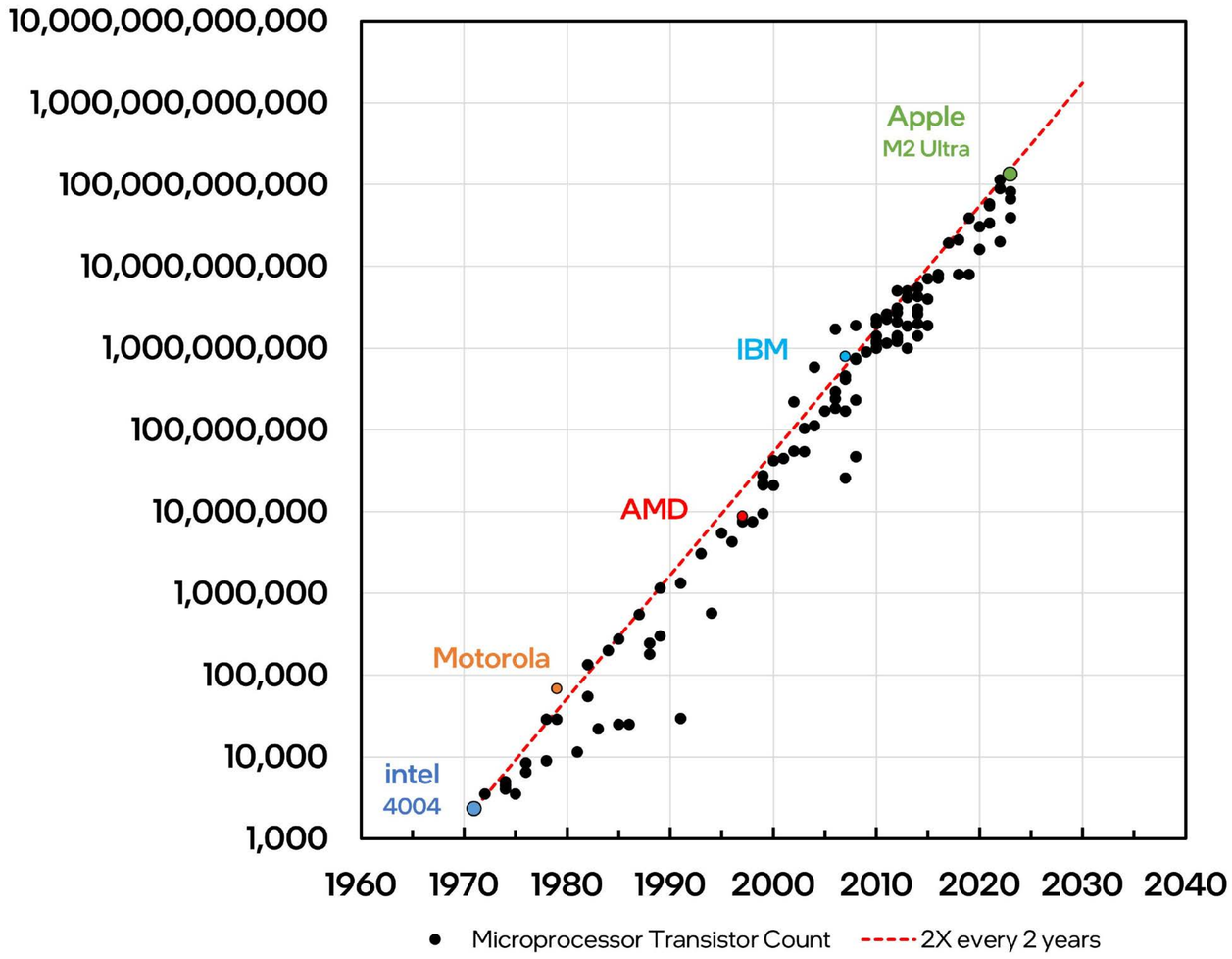
Manufacturing Across Scales

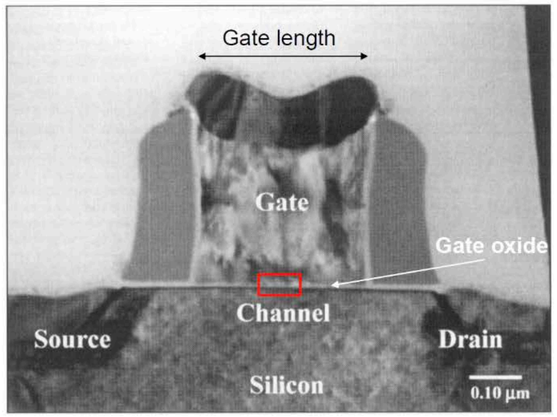


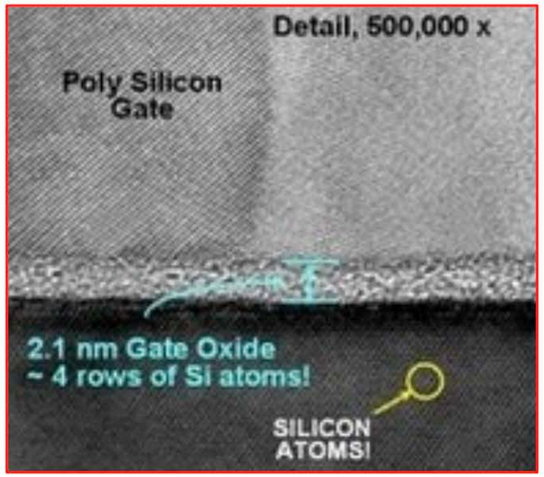
sizes in [nm]



Microelectronics Fabrication







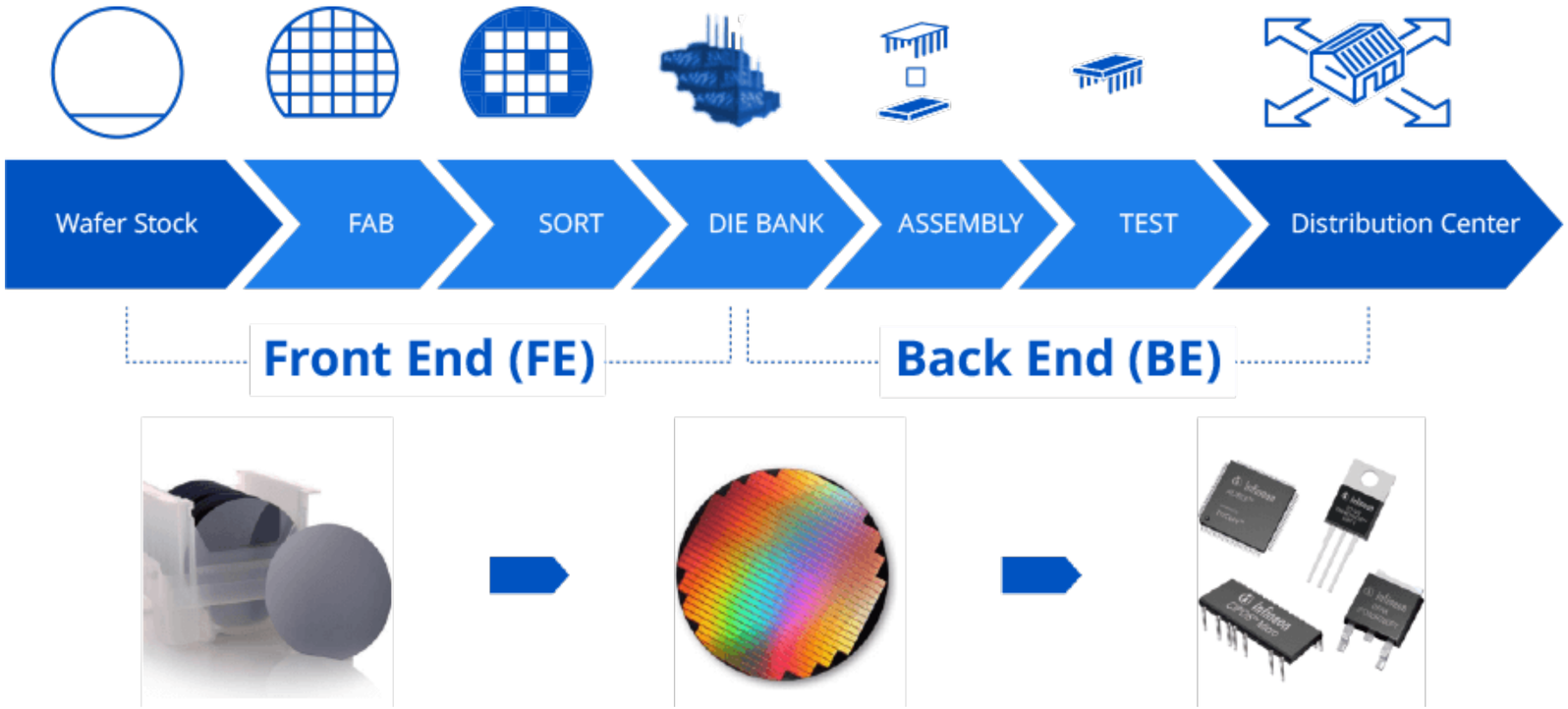
PMOS Transistor

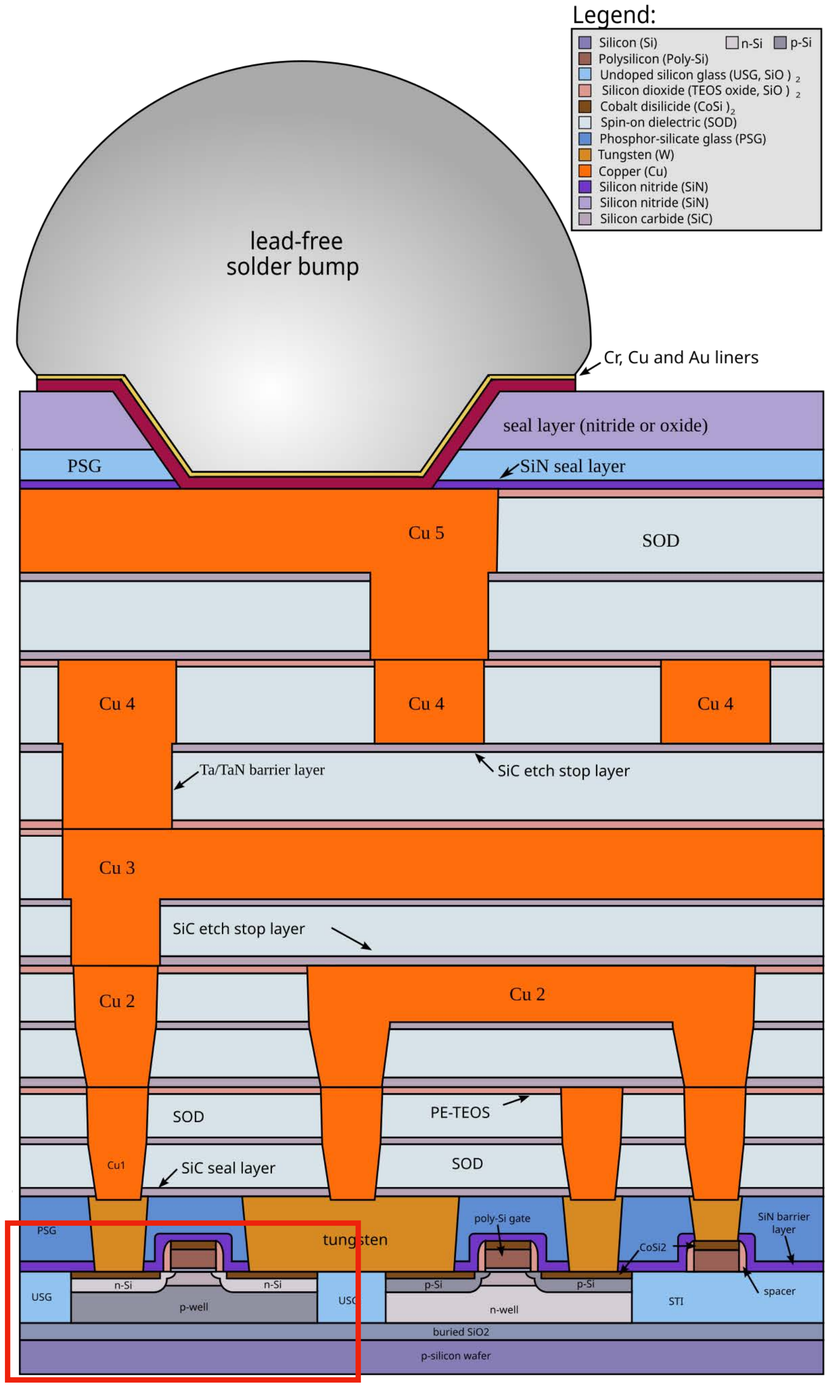
- typical mechanical engineering assembly?

Layered Manufacturing

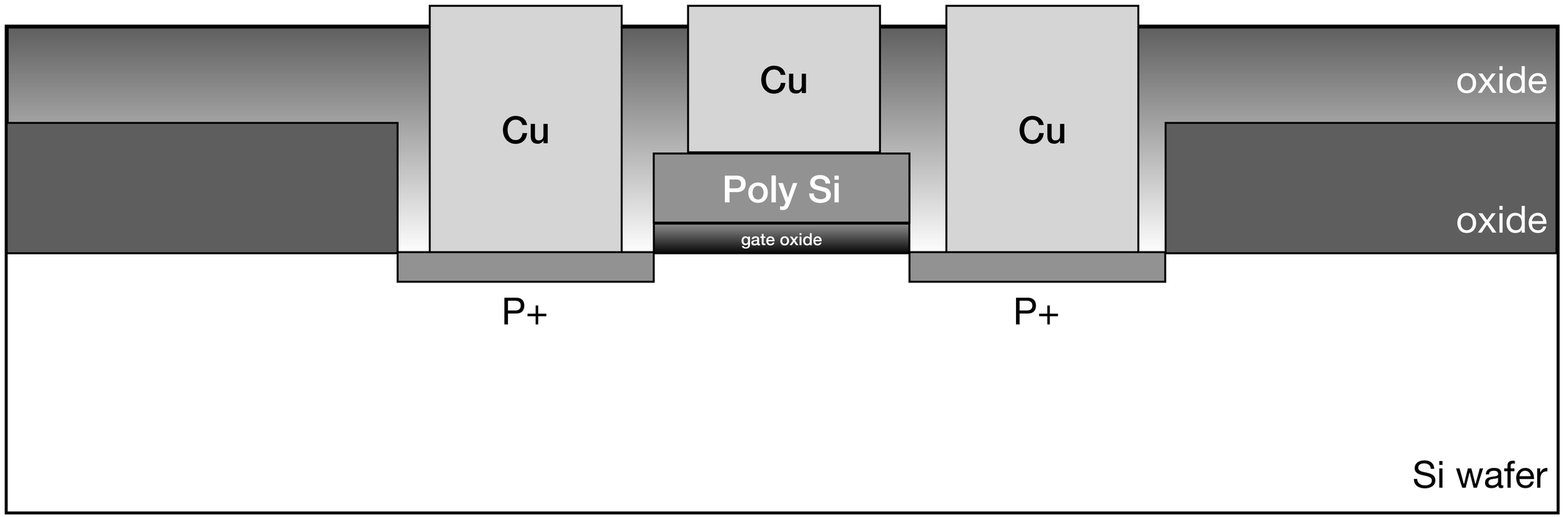
Thin Film Processes: MEMS and Microelectronics

Microelectronics Fabrication





PMOS Transistor

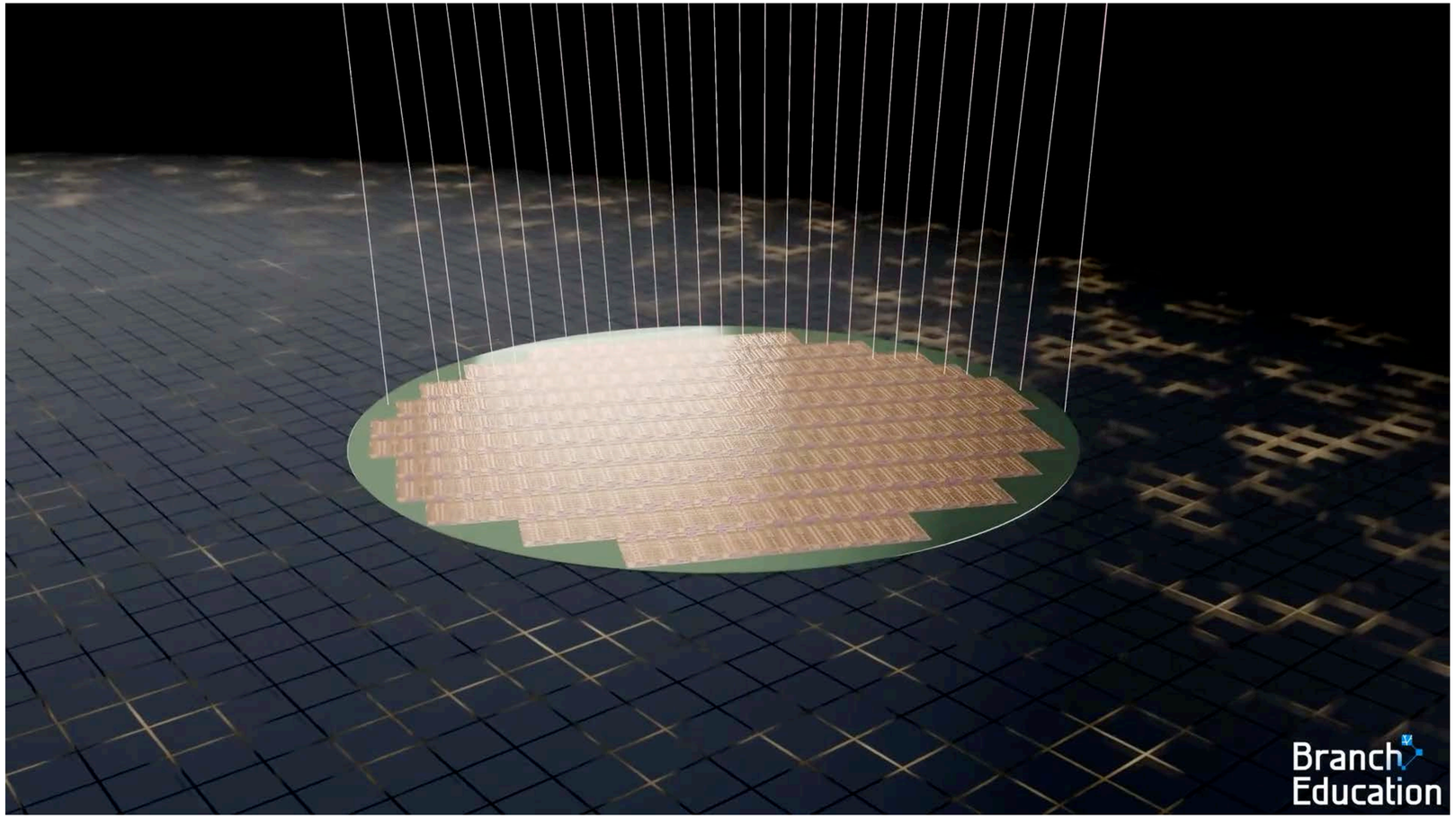


Layered Manufacturing

Thin Film Processes: MEMS and Microelectronics

CPU

- each CPU might have 26 billion transistors



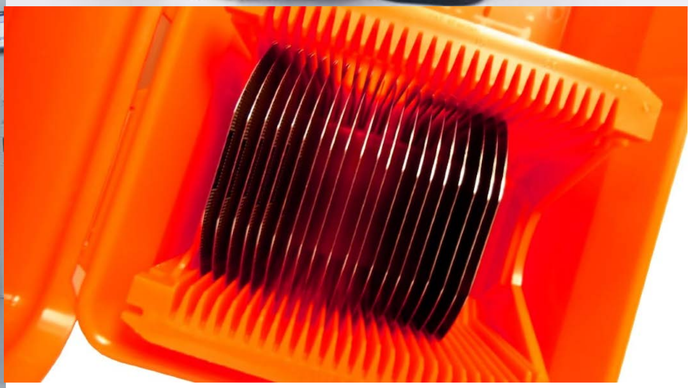
Layered Manufacturing

Thin Film Processes: MEMS and Microelectronics

Semiconductor “Fab” Facility

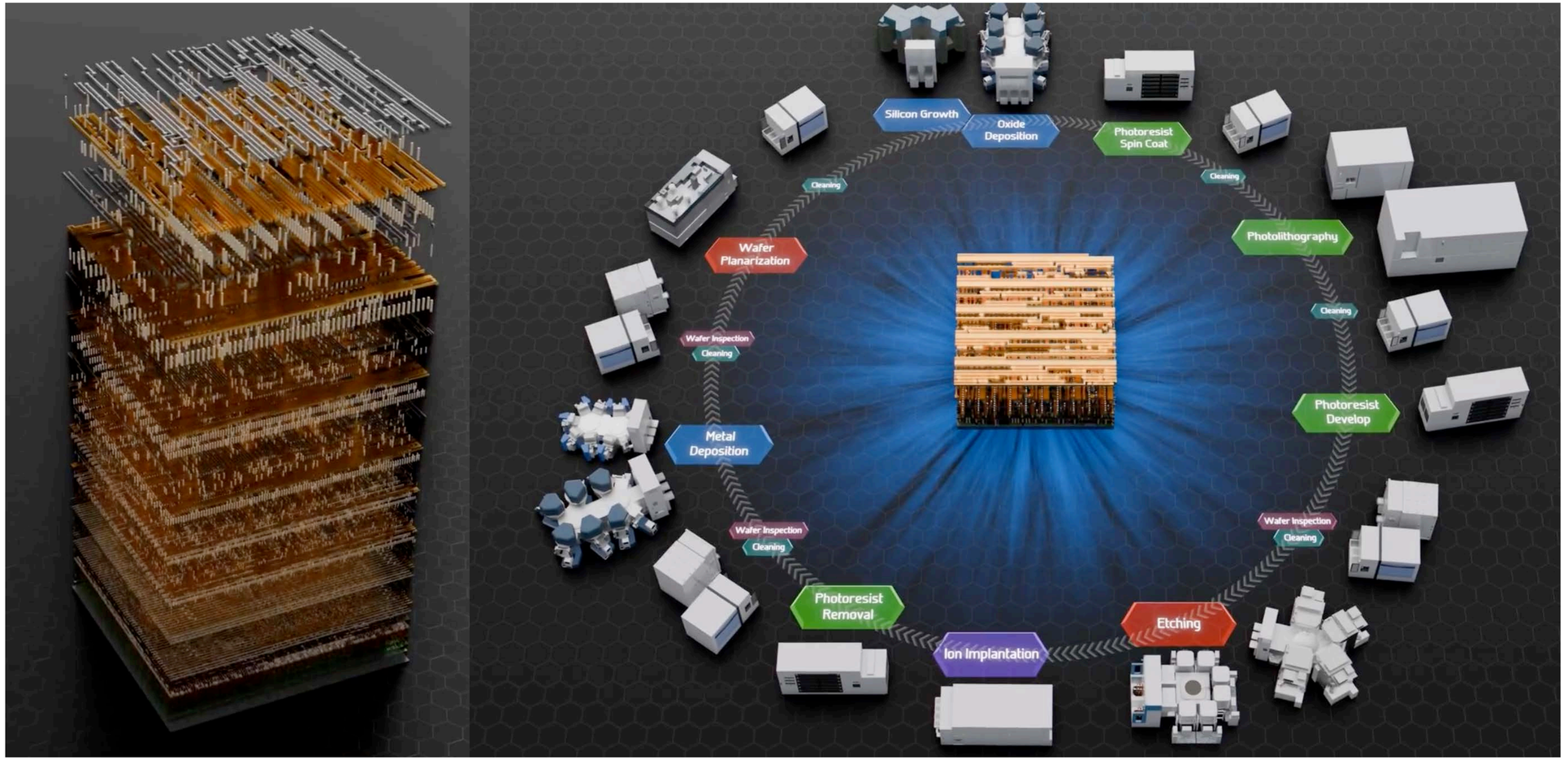
- $20 billion → machines ranging from $3-$200 million (van-bus size!)
- clean room: 8 football fields (minimize static, dust, vibration)
- ~200 major plants globally

Semiconductor “Fab” Facility



FOUP: Front Opening Universal Pod

Generic Process Characteristics



CPU: 80 Layers

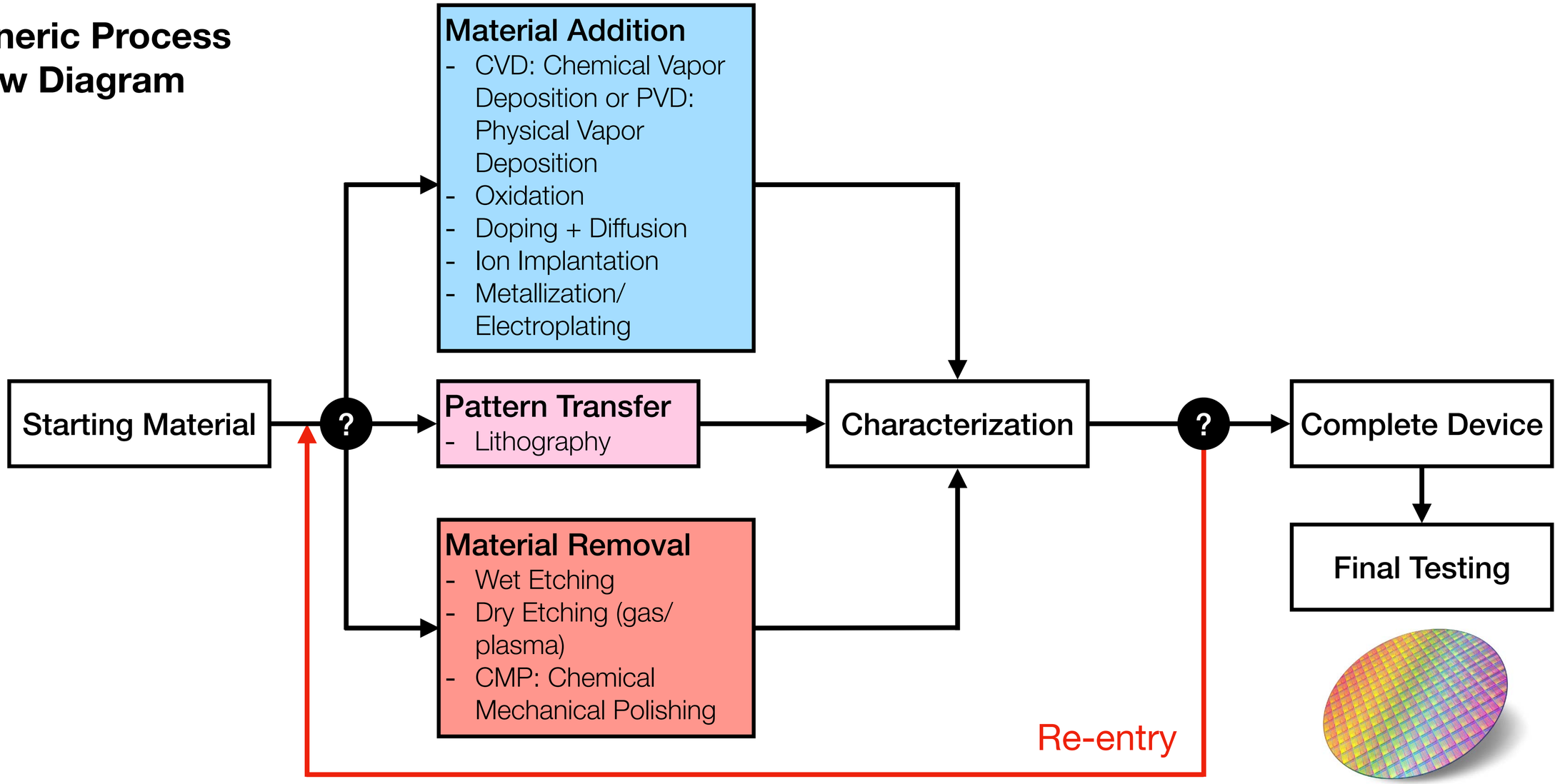
takes 3 months to complete 1 wafer → worth more than weight in gold

Cost

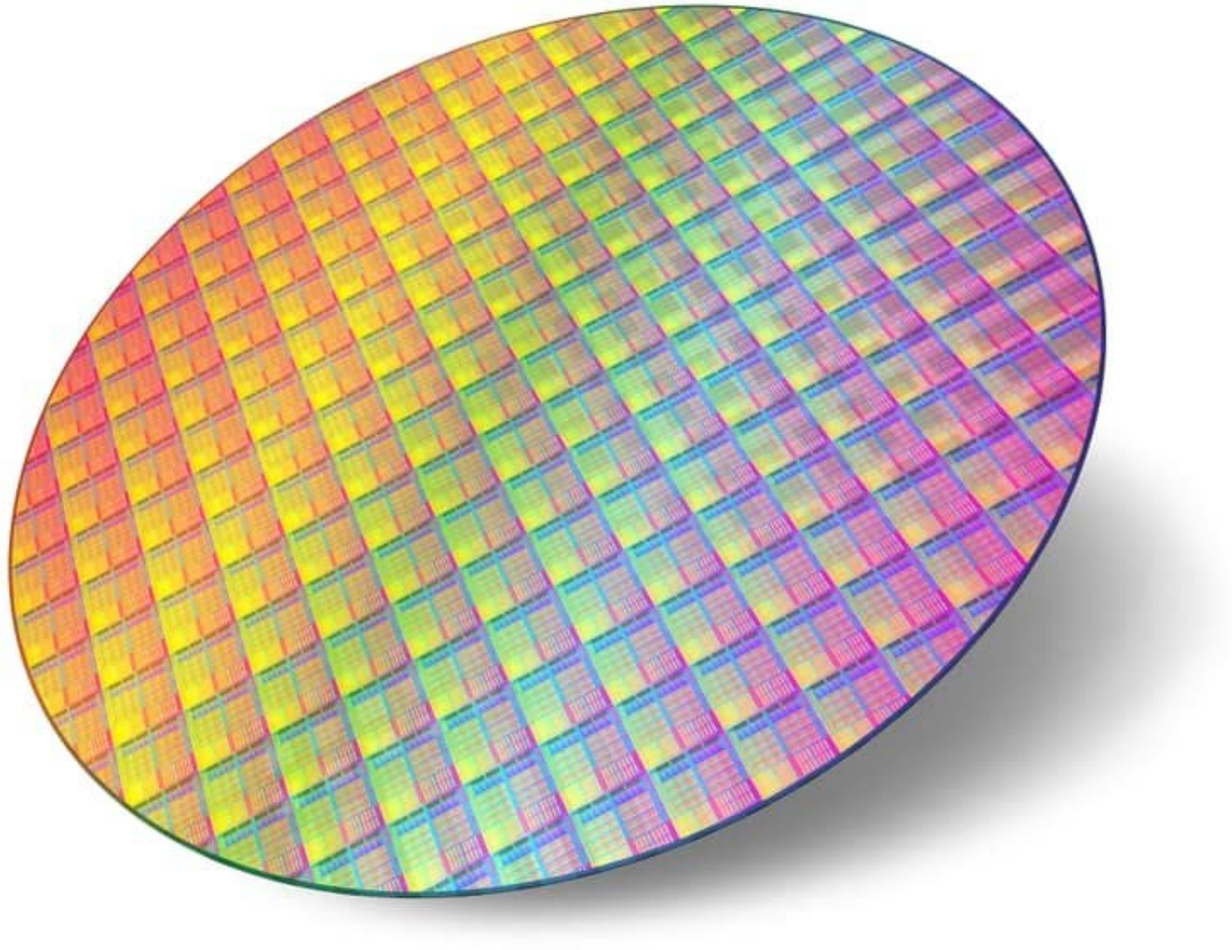
- 1/3 cleaning
- 1/3 photolithography
- 1/3 everything else

SPC: essential!

Generic Process Flow Diagram



Process Preview

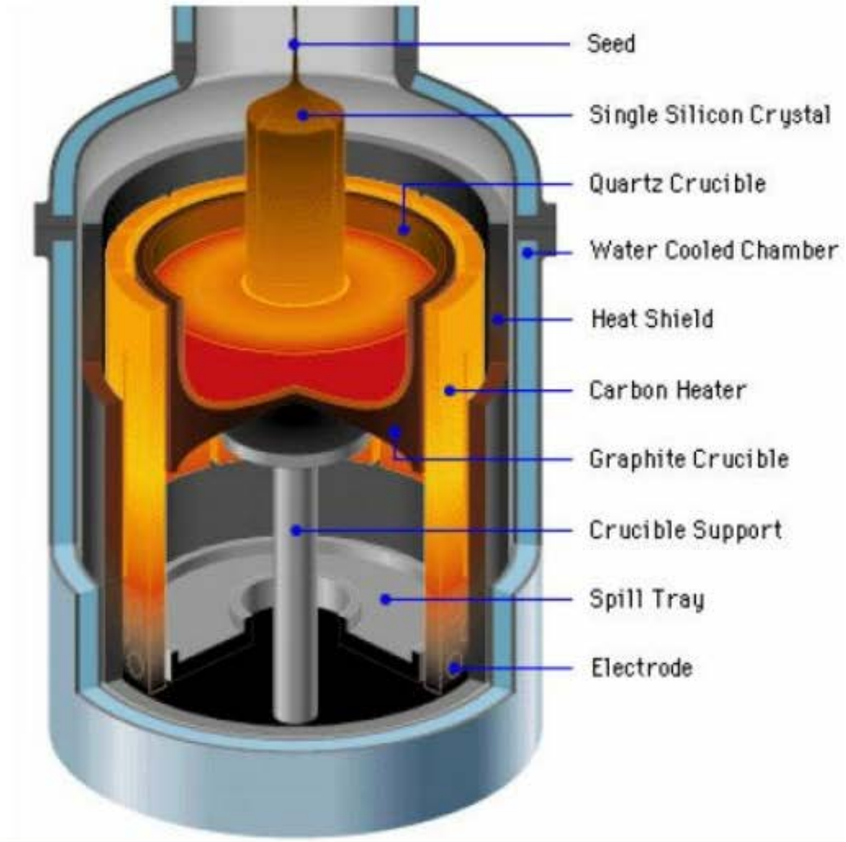


How Chips Are Manufactured

with Optics from ZEISS

ZEISS Semiconductor Manufacturing Technology
www.zeiss.com/smt

Process Flow Example: Starting Wafer



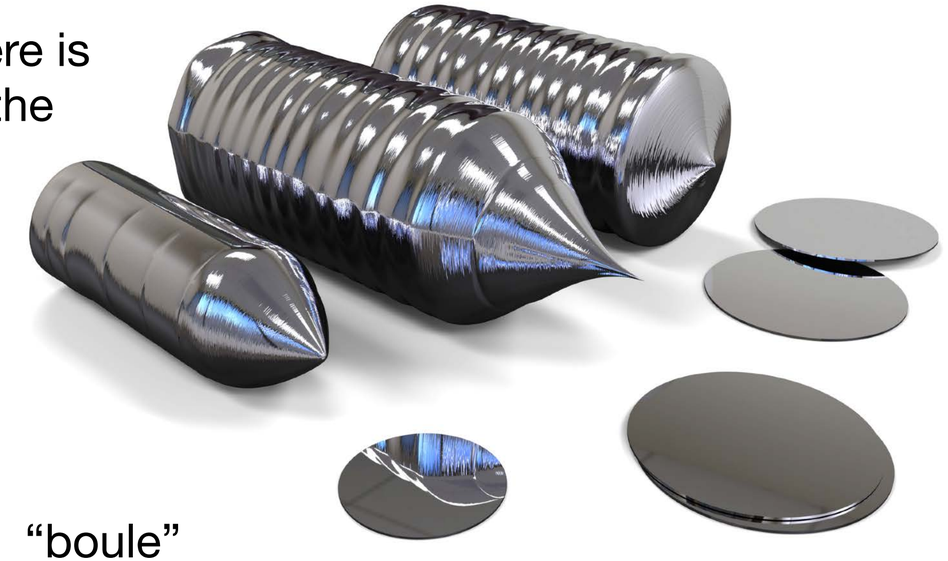
Why Silicon? Need a good **semi**conductor, good fit for manufacturing

alternative: gallium arsenide - better but harder to grow

can alter silicon's lattice structure

Why circular? rotating is part of the mono-crystalline growth process

means there is waste on the edges…



"boule"

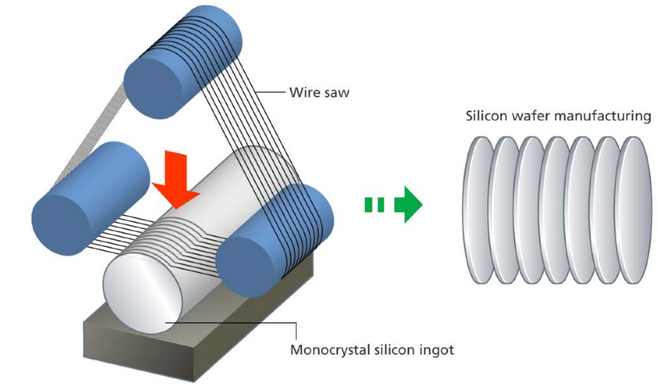
Process Flow Example: Starting Wafer

Starting Wafer

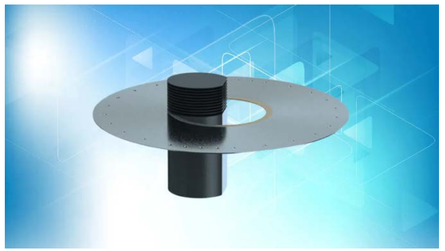
- characterize: electrical measurement

Clean Wafer

- critical resource: water and chemicals for cleaning



wire sawing



ID sawing

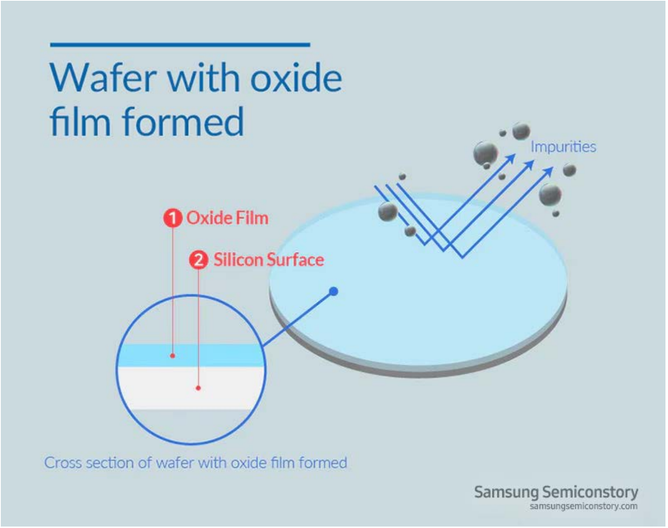
Wafer Diameter: 300mm (~12in)

4” → 8” → **12”** (→ 18”?)

Process Flow Example: Field Oxidation

Field Oxidation

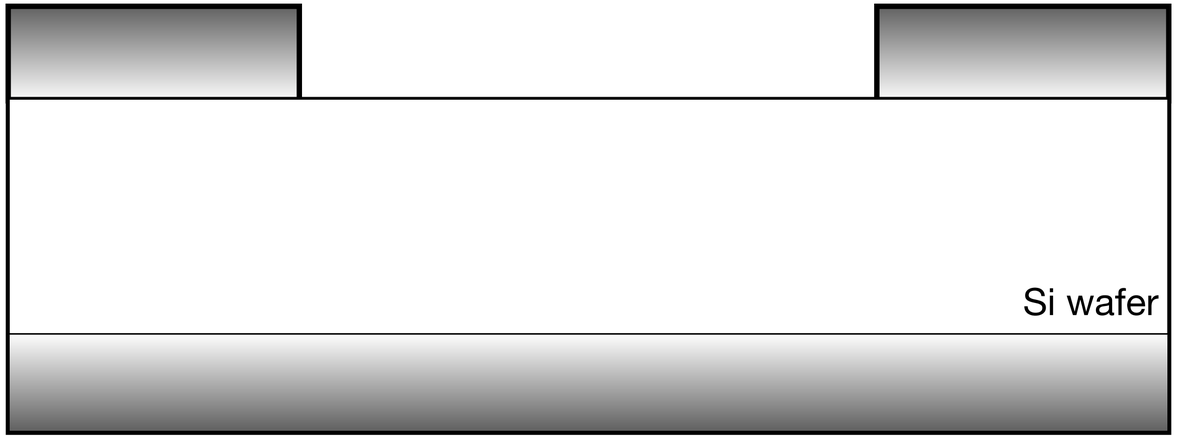
- protect wafer
- furnace: oxygen/water vapor + temperature increase
- some silicon is consumed during this process



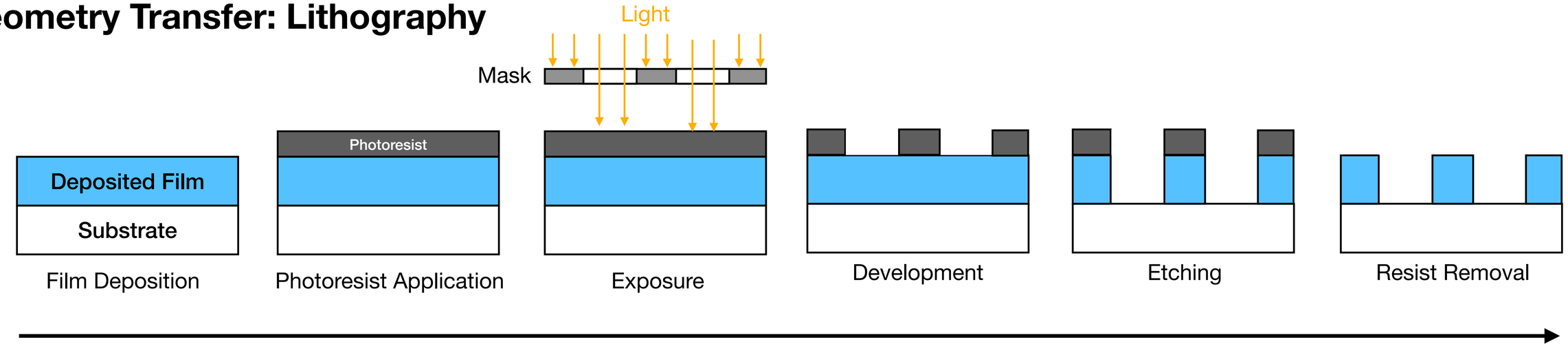
Process Flow Example: Pattern Field Oxide

Pattern the field oxide

- apply photoresist, expose and develop
- etch field oxide
- remove photoresist



Geometry Transfer: Lithography

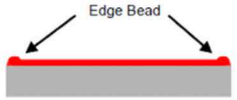


Lithography: Photoresist Application

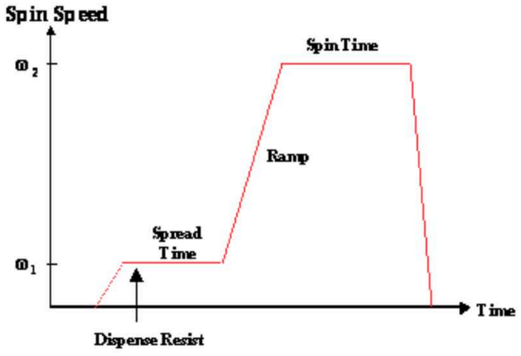
1. EQUILIBRIUM STAGE
(stopped)

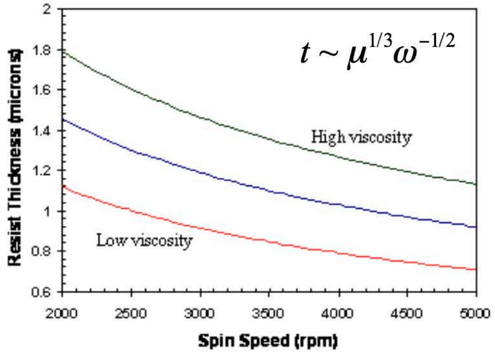
2. WAVE-FORMATION STAGE
(~ 2 revolutions)

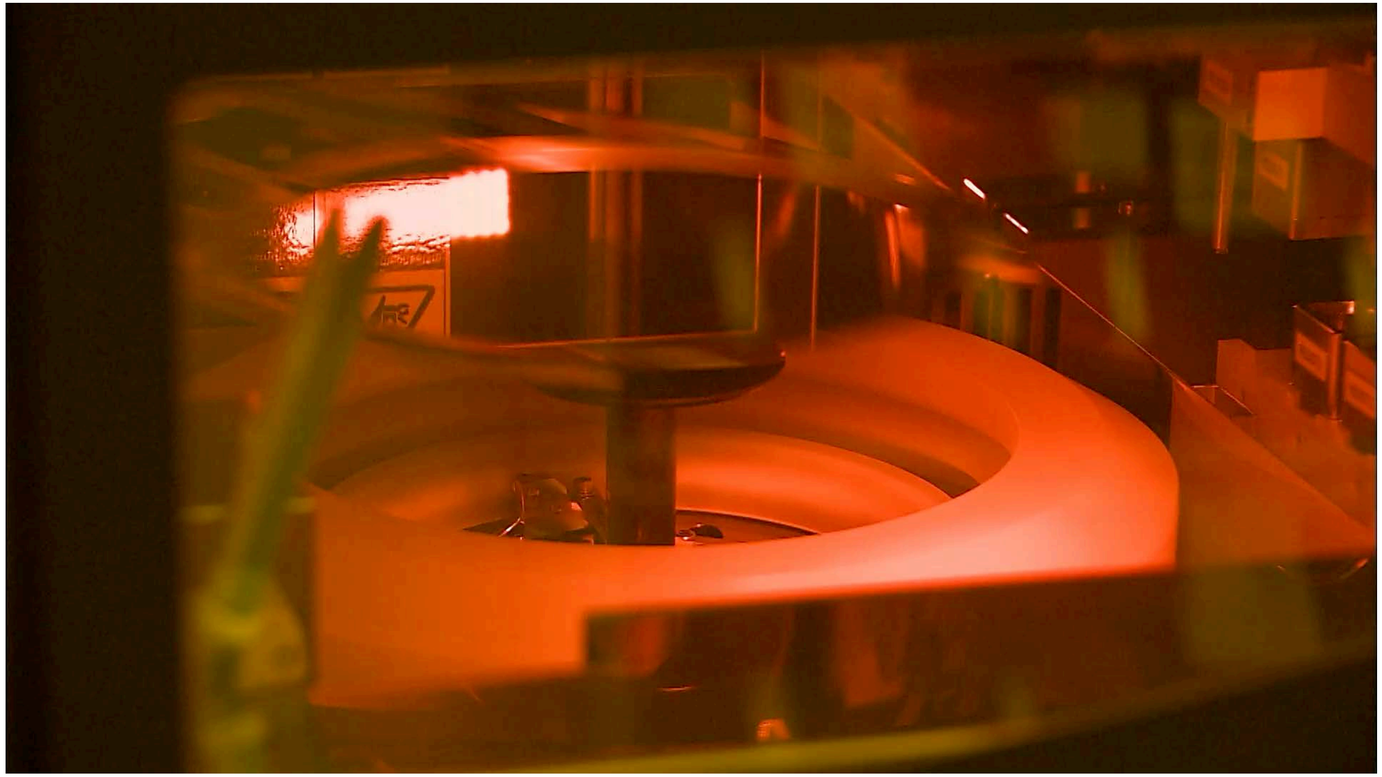
3. CORONA STAGE
(~ 30 revolutions)



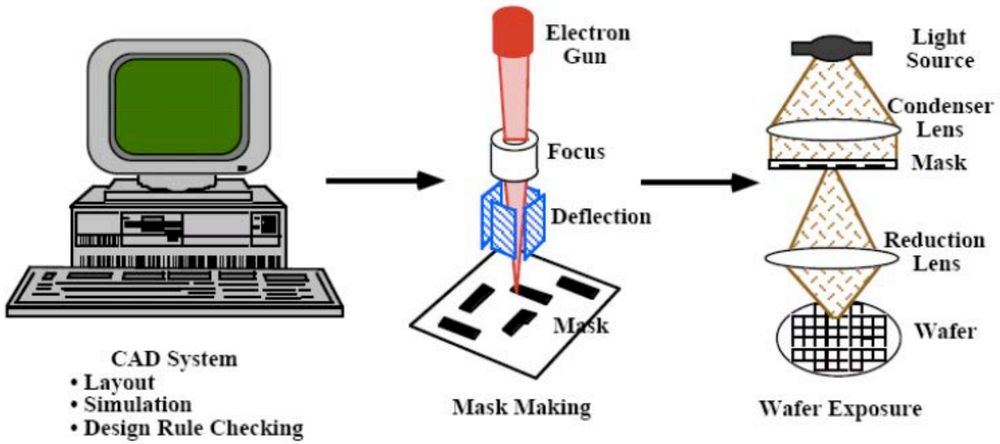
4. SPIRAL STAGE
(~ 1000 revolutions)



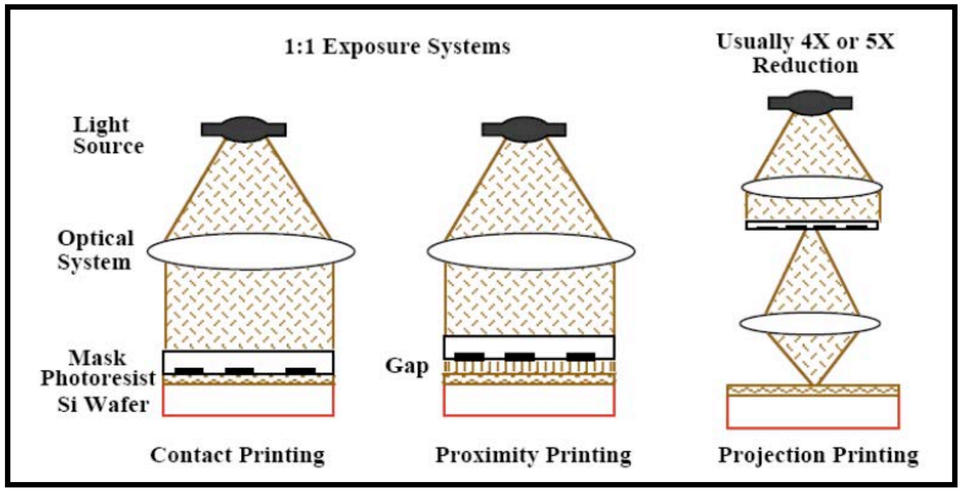


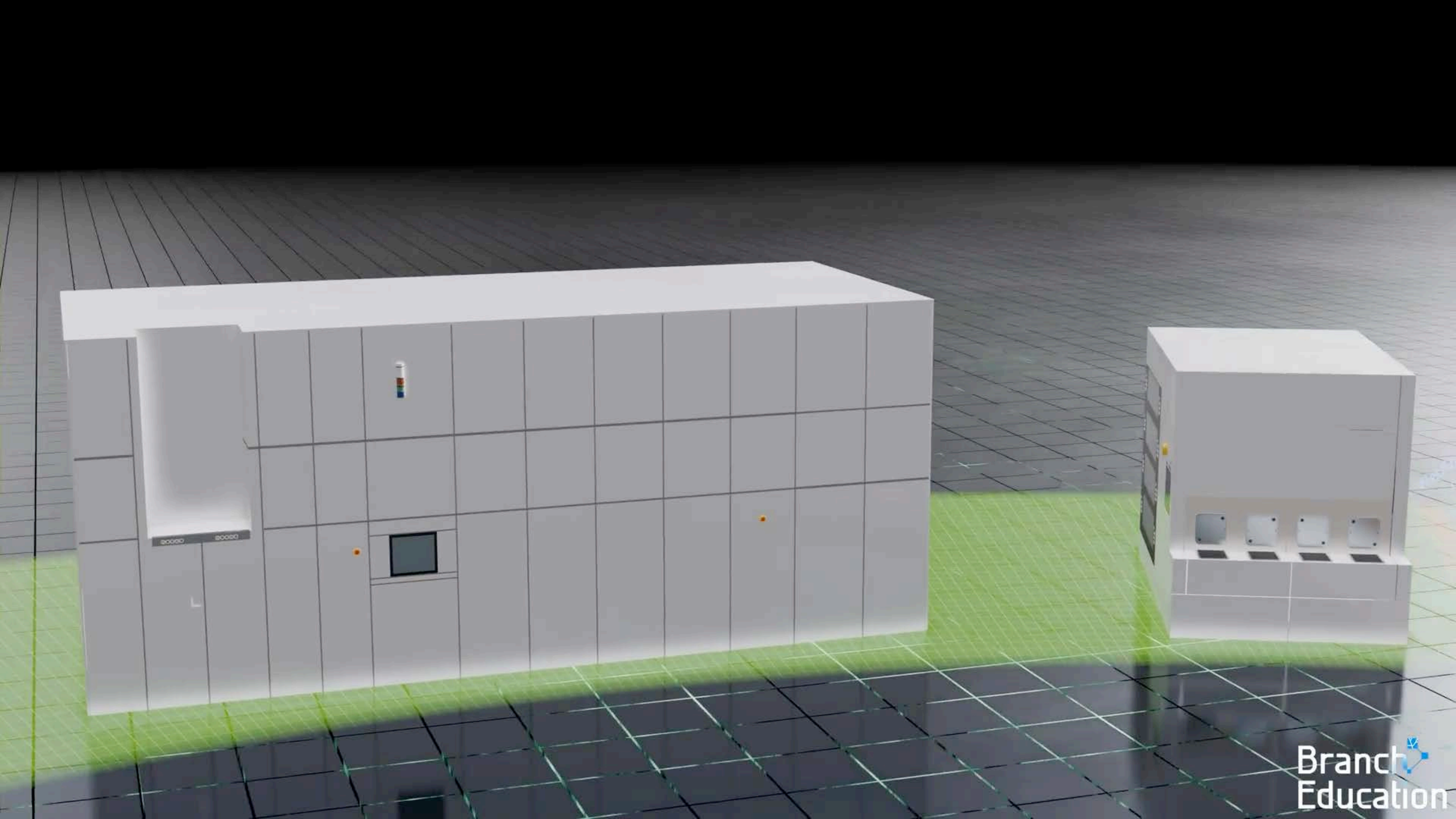


Lithography: Patterning



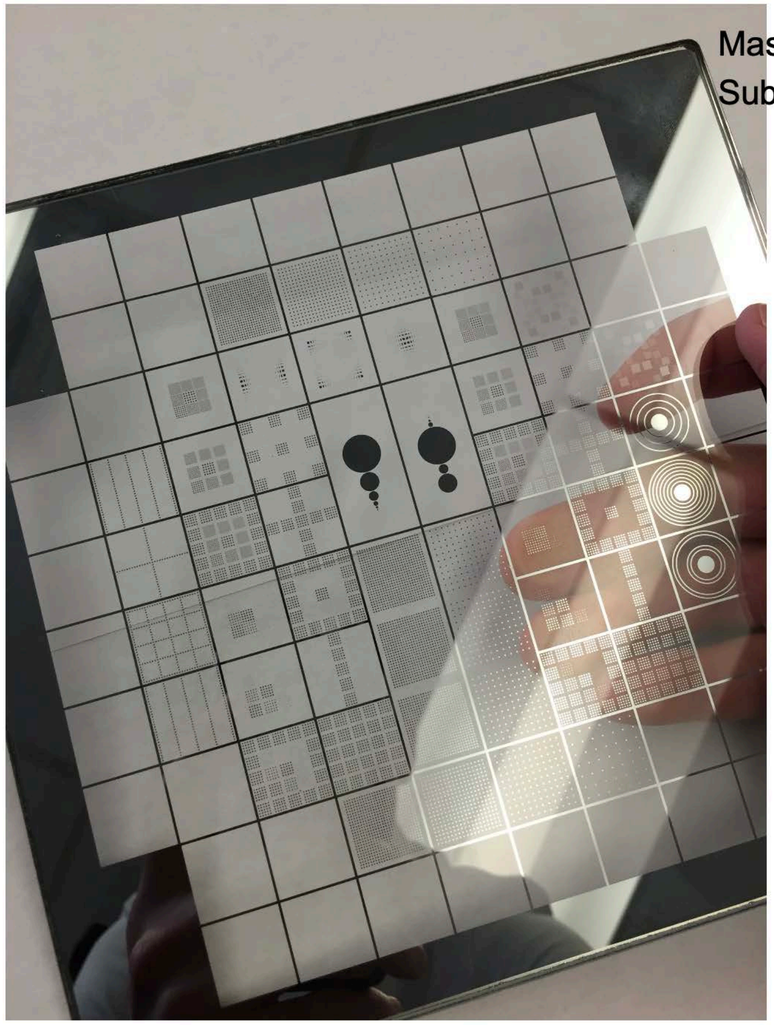
CAD tooling part




Branch
Education

Lithography and Patterning: Photo Masks

Could be using 80 masks for 80 layers

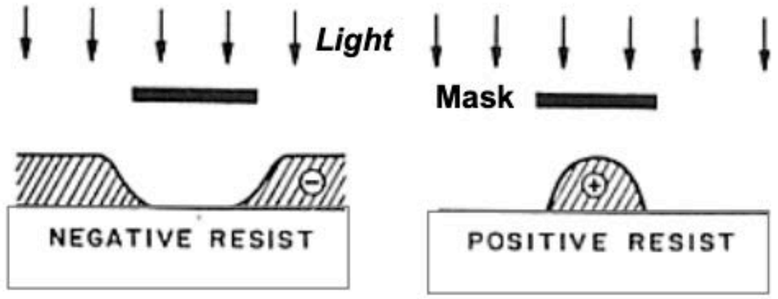


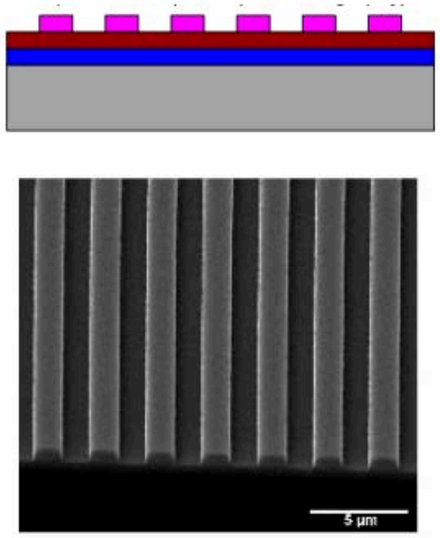
Mask patterns = Chrome

Substrate = Glass (soda-lime or quartz)

Lithography and Patterning

EUV Light: Extreme Ultra Violet





"Rayleigh's Resolution Criterion"

Smallest resolvable feature *x*:

$$x = k\frac{\lambda}{NA}$$

Where:

λ=wavelength of light

NA = Numerical aperture of the optics

k = process-dependent constant (<1)

Lithography and Patterning: Light Generation

13.5

NANOMETERS

...is the wavelength of the extreme ultraviolet (EUV) light that is created, which facilitates the manufacture of structural sizes of less than 10 nanometers.

50,000

TIN DROPLETS PER SECOND

... are hit by the TRUMPF Laser Amplifier, to create EUV rays for substrate exposure.

100,000,000

TRANSISTORS PER SQUARE MILLIMETER

... and more can be placed on a single microchip due to EUV lithography - which is almost inconceivable.

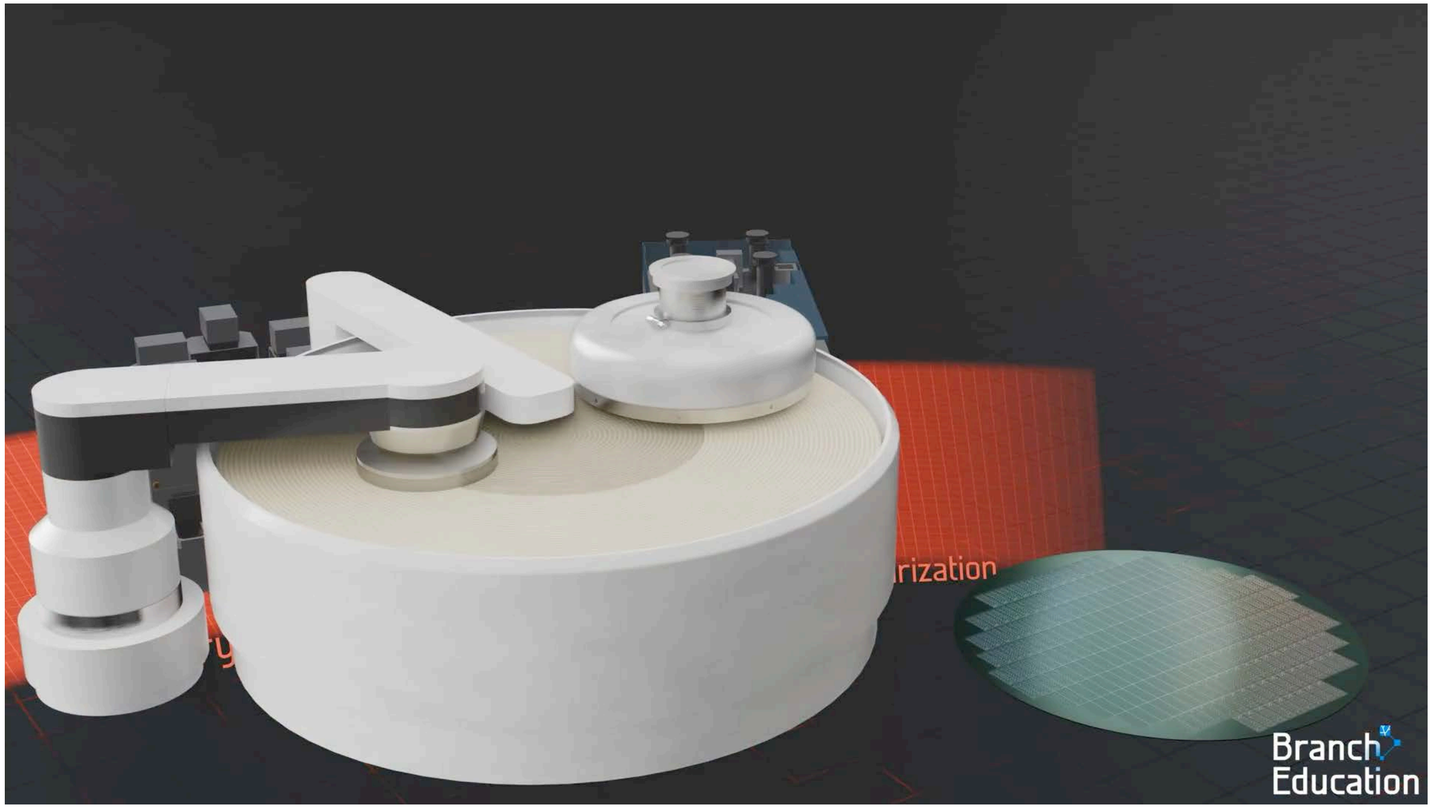
Planarization

finer wavelength of light → shallower depth of focus

- after material addition, you do not have a flat surface
- these steps compound in height
- needs to be **really, really, really** flat for lithography

polishing is needed in order to flatten the wafer

- perfect for mechanical engineers!



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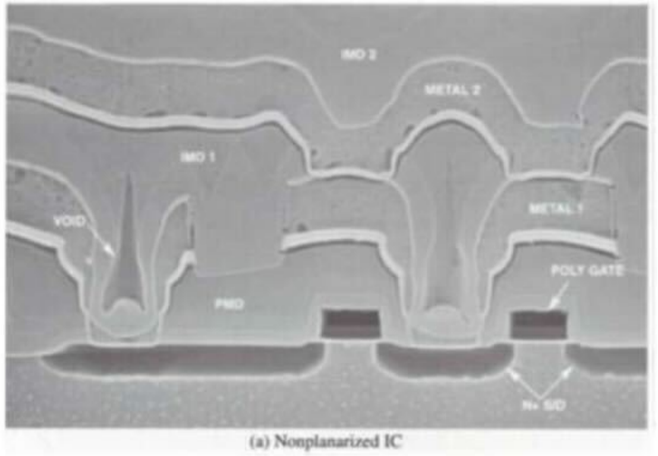
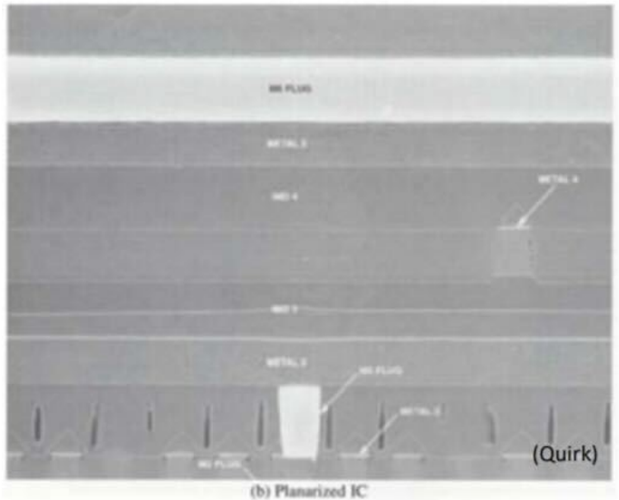


(a) Nonplanarized IC

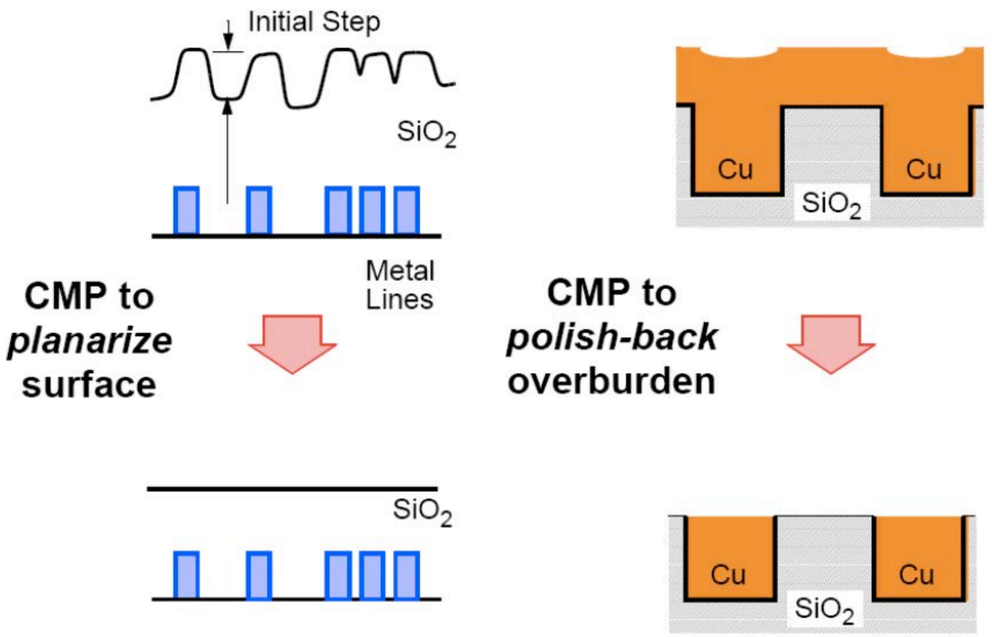
pre-CMP

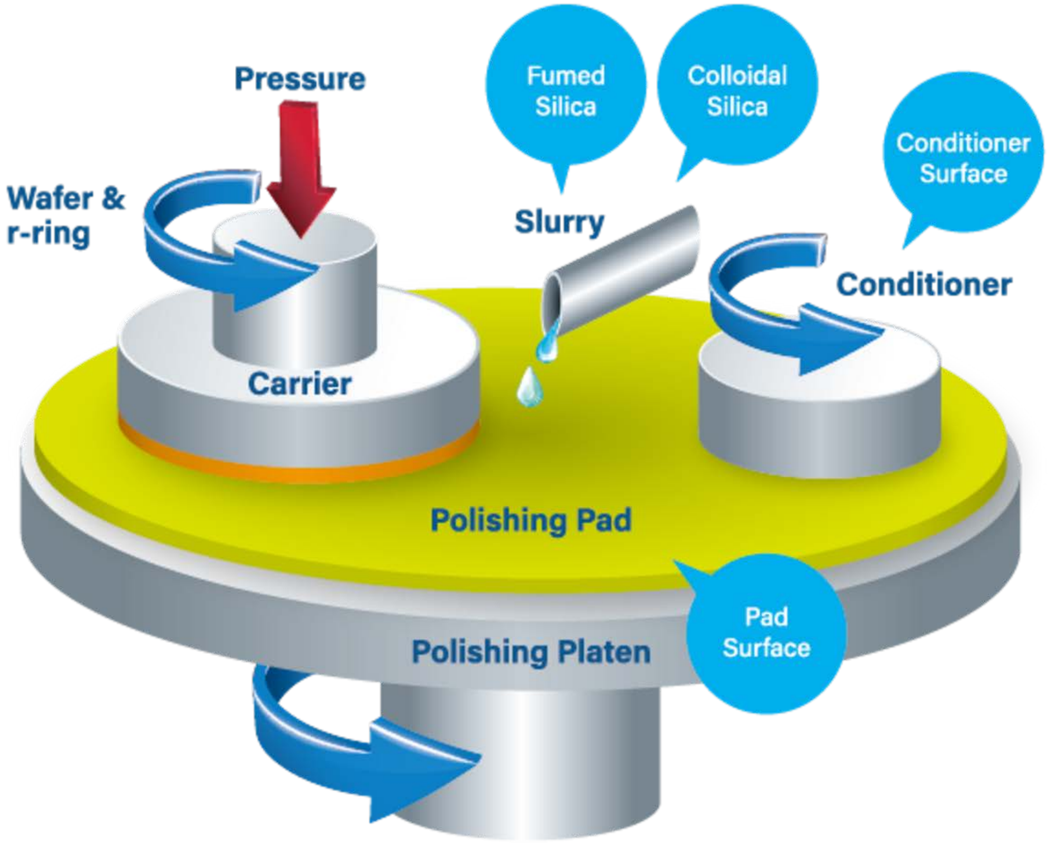


(b) Planarized IC

post-CMP

Chemical Mechanical Polishing





silicon is hard, and e.g. copper is relatively softer

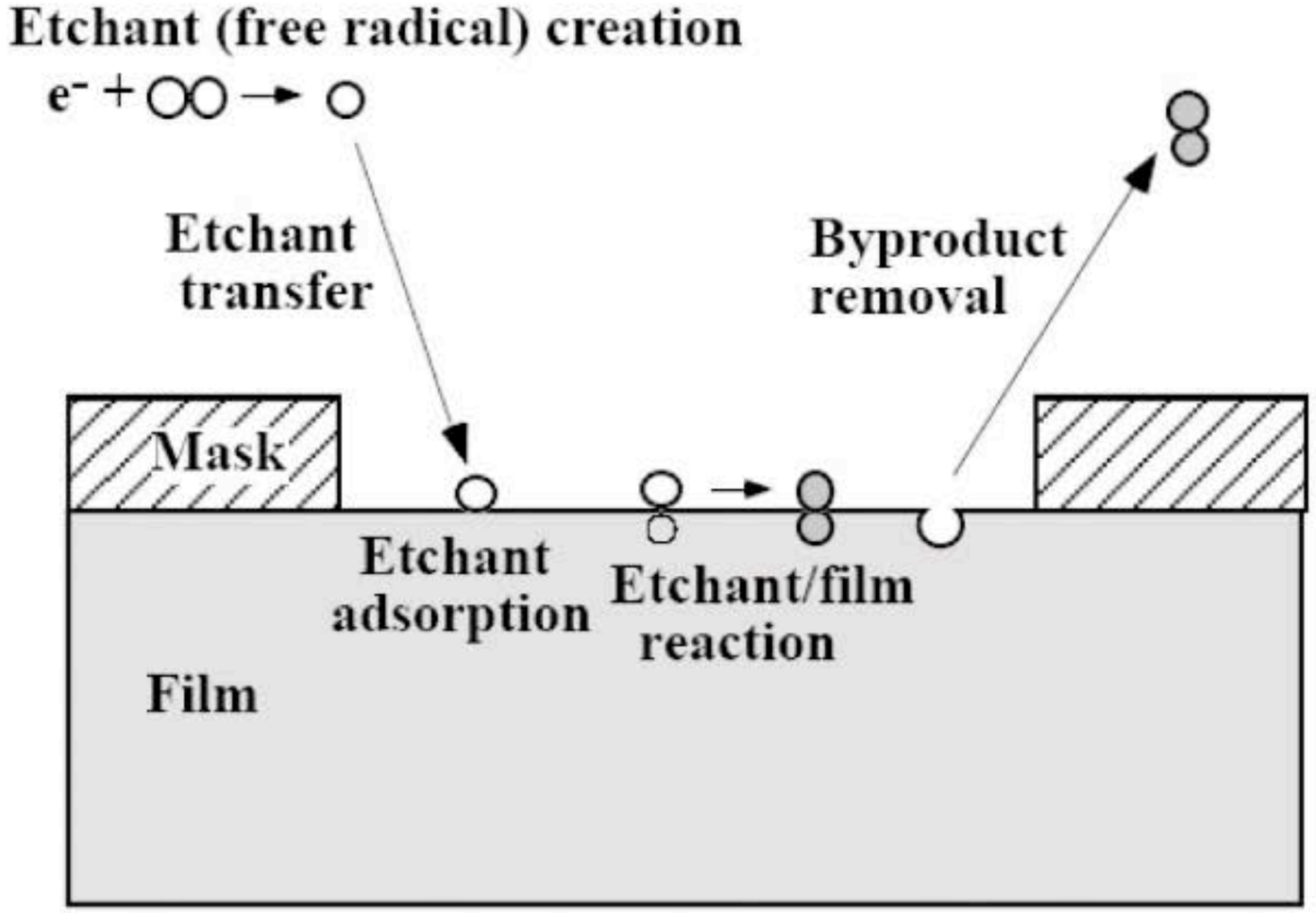
- balancing act: polish both without over/under polishing

slurry: abrasive chemical suspended in a solution

pads: porous to hold slurry and supply mechanical energy

material removal: mechanical + chemical actions

Etching: Process

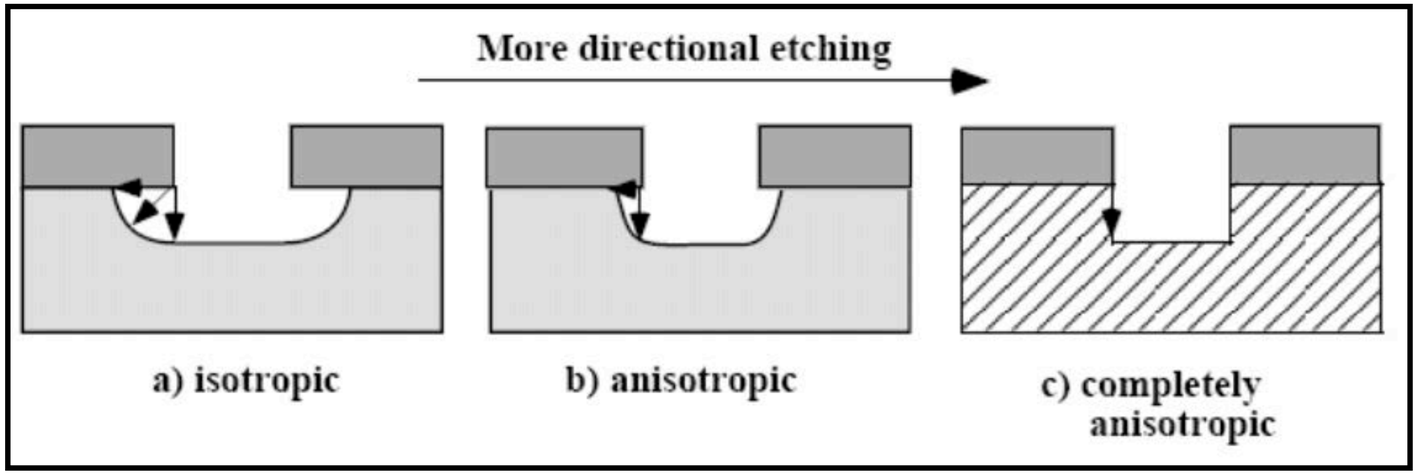


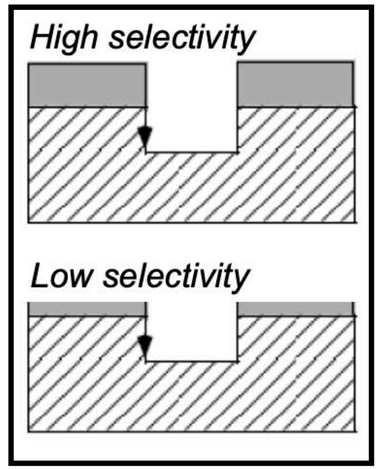
Etching: Process

must figure out **selectivity** (comes from chemistry) and **directionality** (comes from physical processes)

- want good control of both

wet dry

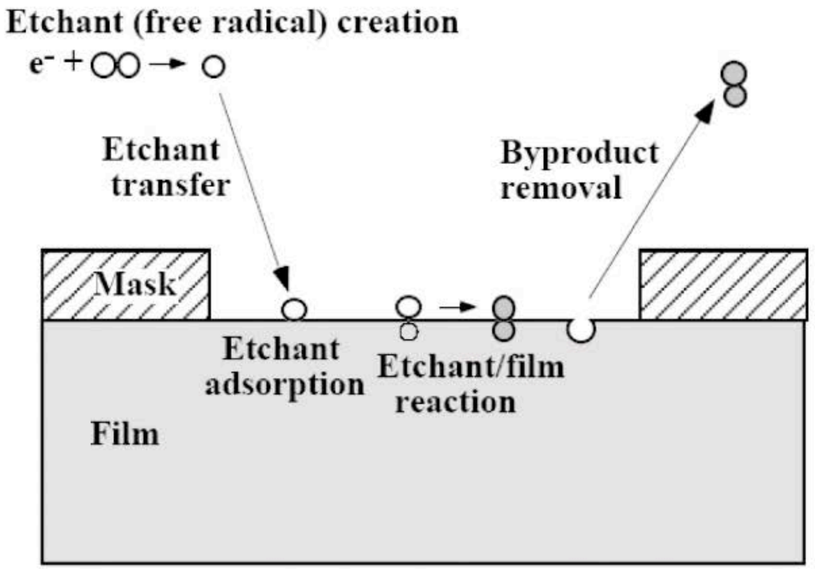


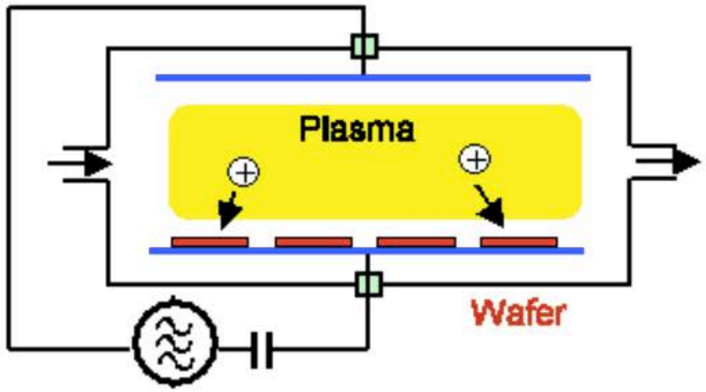


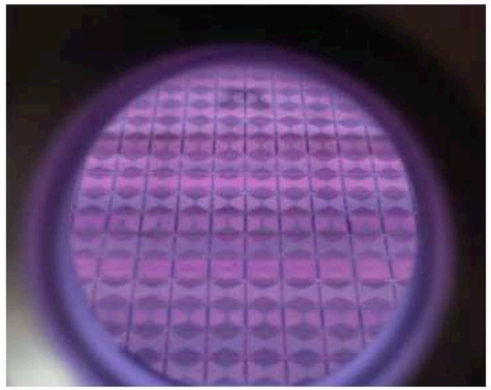
Plasma Etch: Surface Chemistry

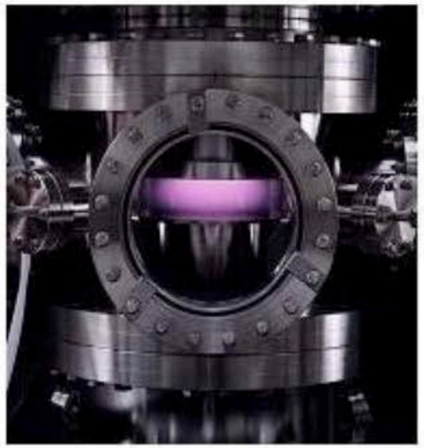
etching can be done **dry** or **wet**

- dry etching: use of plasma





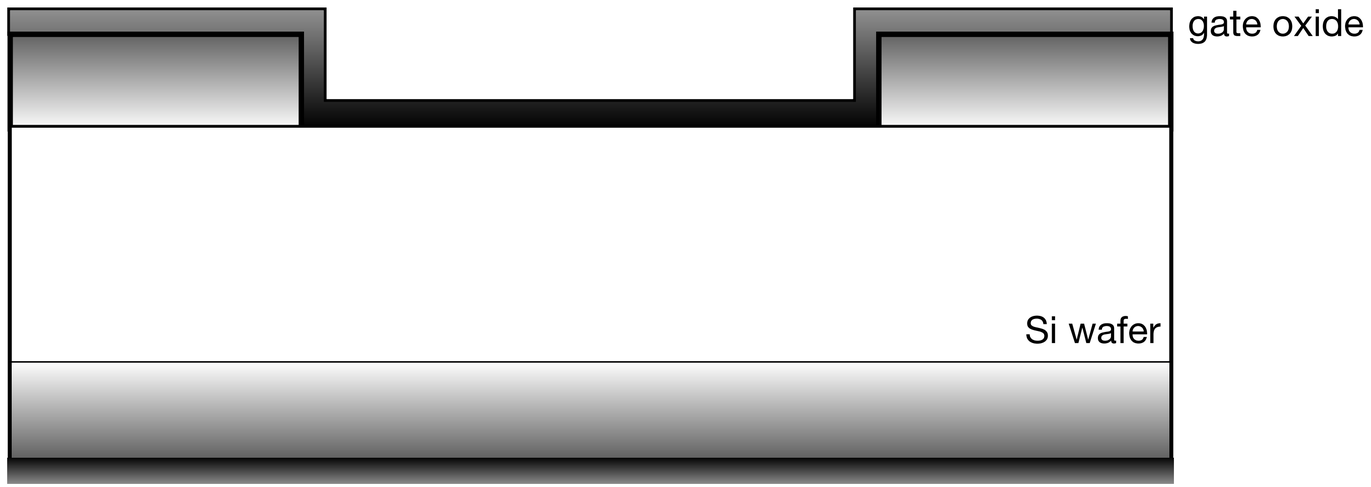




Process Flow Example: Gate Oxidation

Gate: critical for electrical performance of the transistor

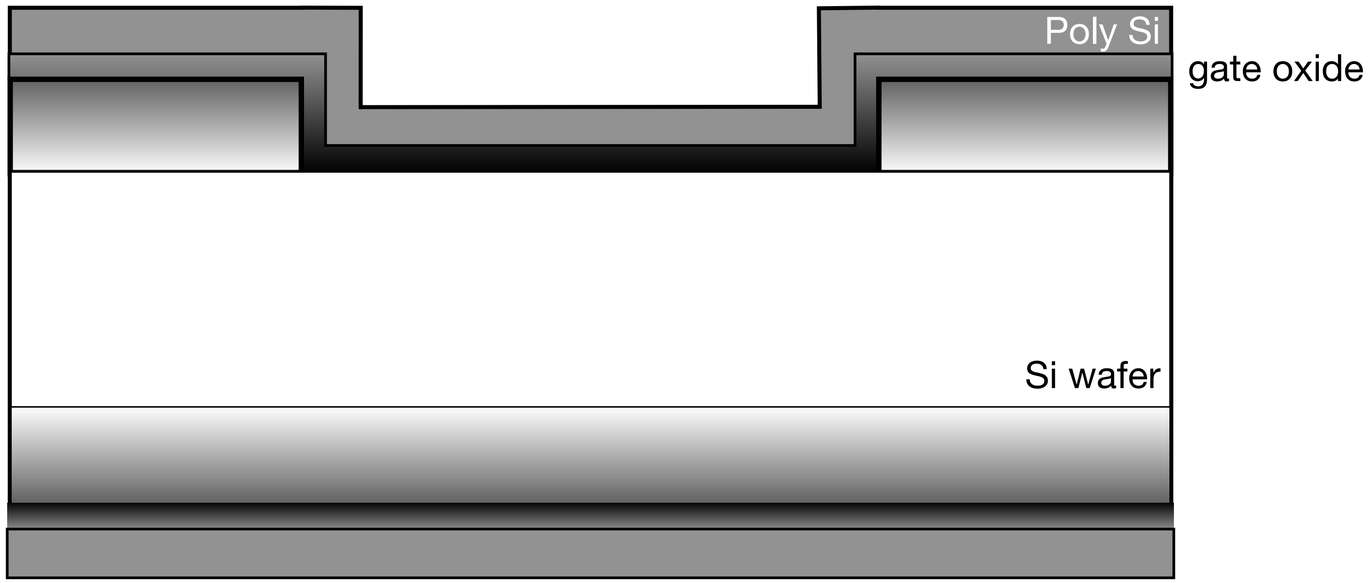
- need higher quality oxide than previous steps
- high purity from a well controlled process



Process Flow Example: Poly Si Deposition

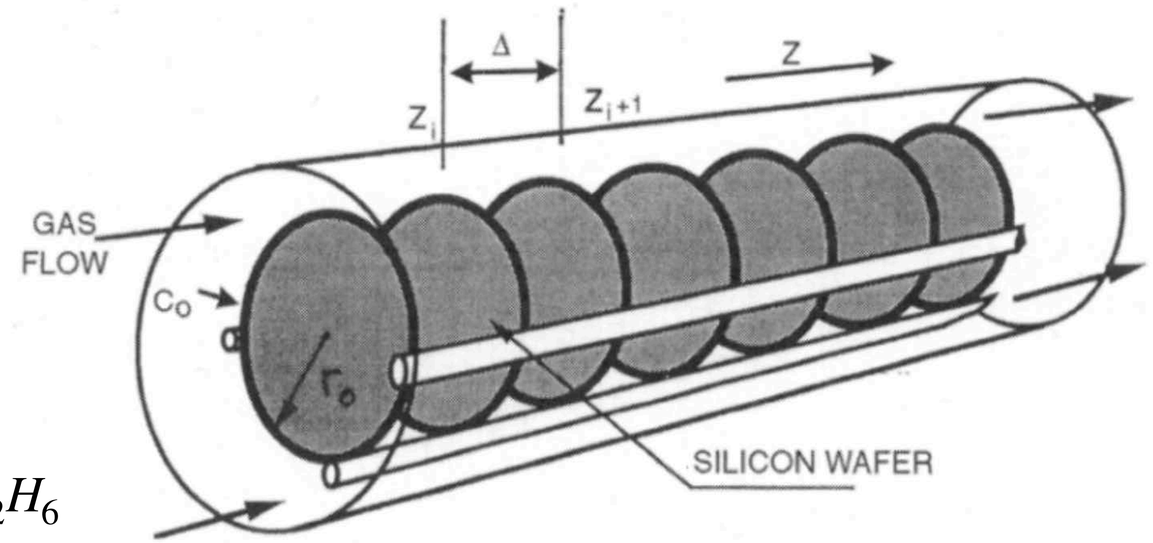
Poly Si Deposition

- polycrystalline silicon: different material properties from starting wafer
- both Poly Si and Gate Oxide applied with CVD



Chemical Vapor Deposition

SiH_4
N_2
HCl
H_2
PH_3, AsH_3, B_2H_6



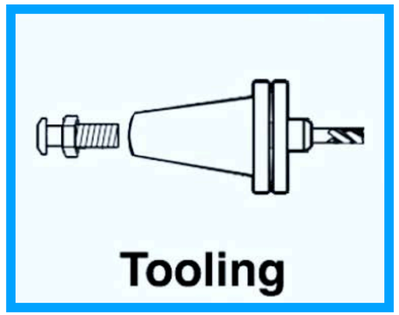
H_2
$SiCl_2$
$SiCl_4$
SiH_2Cl_2
$SiHCl_3$

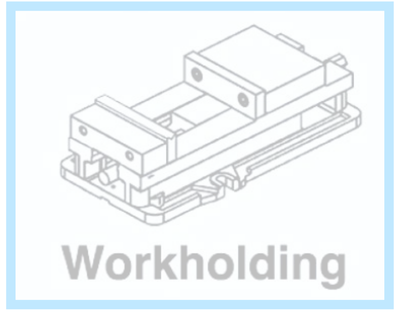
CVD: deposition method that uses a chemical reaction to deposit materials from gaseous precursors

- precursors: trade secrets 🤫
- versatile
- conformal (coats surface)
- good for thicker coatings

PVD: deposition where a material (typically a metal) is vaporized and flows such that it can condense on the substrate

- good for thinner coatings





Tool Coatings

- increase wear resistance
- increase oxidation resistance
- reduce friction
- increase resistance to metal fatigue
- increase resistance to thermal shock

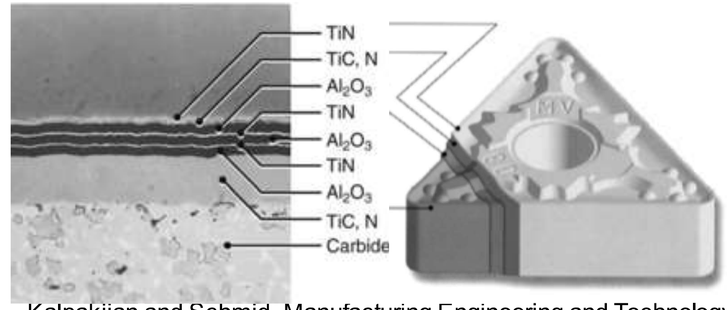
Layers: 2-20 µm thick

TiN: low friction

TiCN: wear resistance

Al_2O_3: high thermal stability

Carbide: hardness and fracture toughness

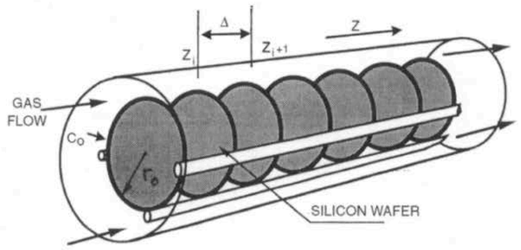


Kalpakjian and Schmid, Manufacturing Engineering and Technology.
from DeGarmo's Materials & Processes in Manufacturing (10th Edition) by Black and Kohser, © Wiley (2008).

Examples:

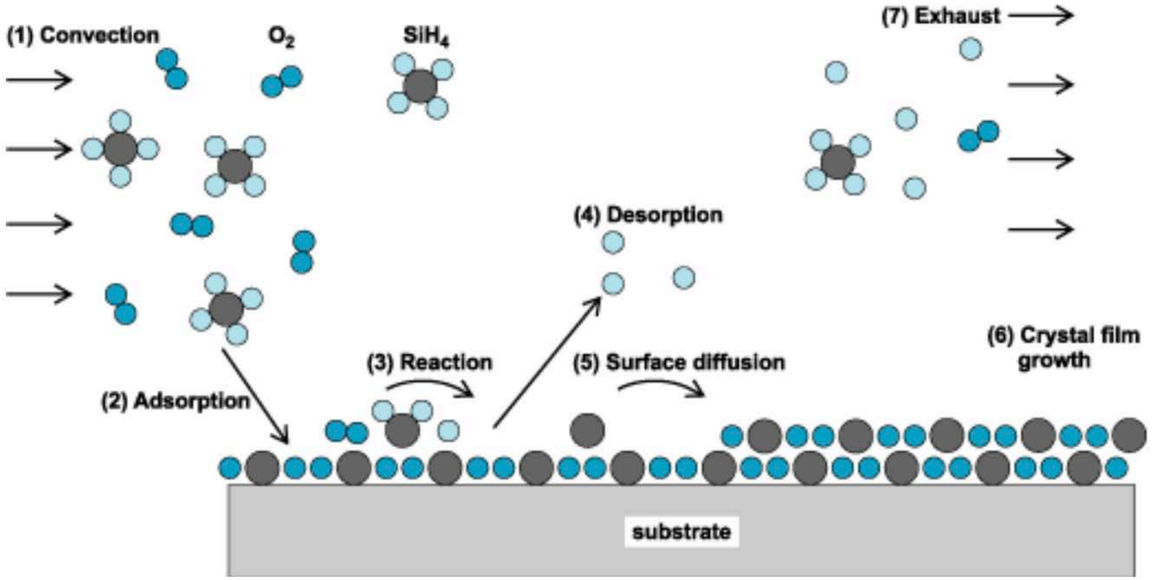
- TiN (a basic yellowish coating that has fallen out of wide use)
- TiCN (a popular bluish-grey coating)
- TiAlN and AlTiN (an extremely popular dark purple coating)
- TiAlCrN, AlTiCrN and AlCrTiN (PVD coating)
- PCD: polycrystalline diamond

Chemical Vapor Deposition



$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \uparrow$$

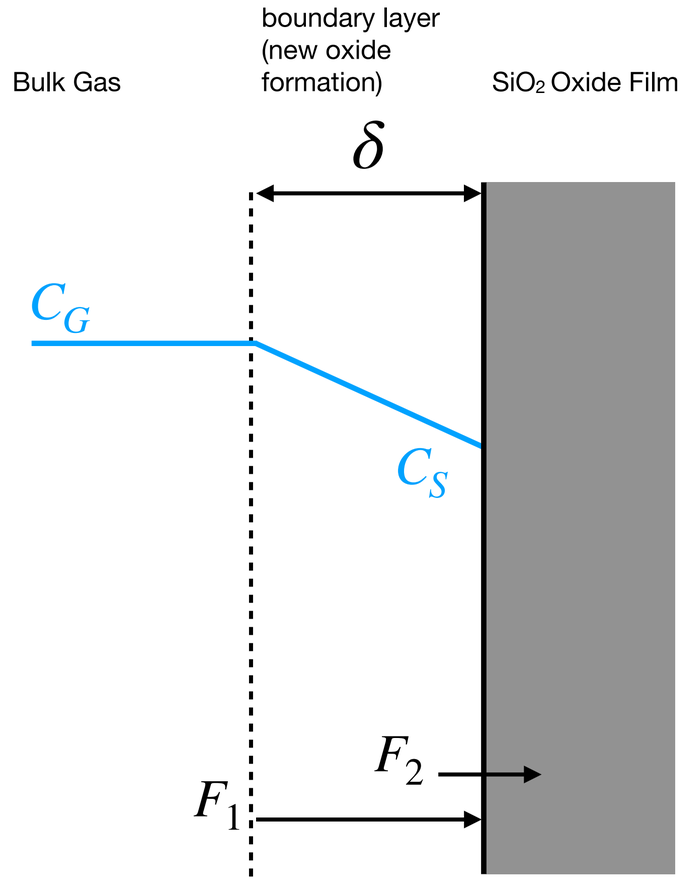
gas (reactant) · gas (reactant) · solid (SiO_2) · 350°C-500°C



Generic: 2AB (gas) → 2A (solid) + B_2 (gas)

Chemical Vapor Deposition: Rate (Diffusion vs Reaction)

"Deal-Grove Model"



Diffusion Flux $F_1 = h_G(C_G - C_S)$

Reaction Flux $F_2 = kC_S$

Steady State $F_1 = F_2$

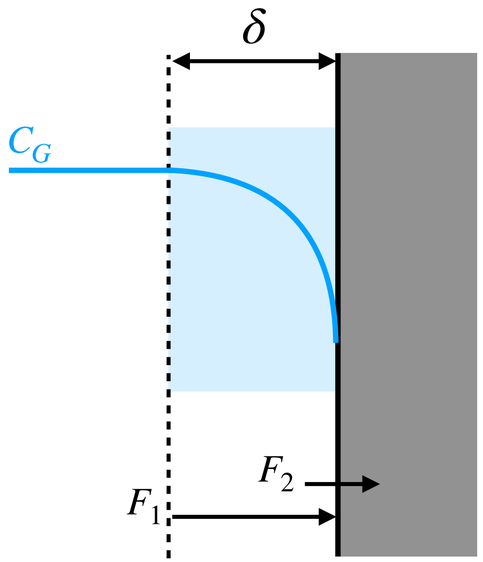
$$kC_S = h_G(F_G - C_S) \rightarrow C_S = \left(\frac{h_G}{k + h_G}\right) C_G$$

Growth Rate $$v = \frac{kC_S}{N} = \frac{C_G k h_G}{N(k + h_G)}$$

h_G: mass transfer coefficient (diffusivity of gas/δ)
C_G: concentration of reactant (oxy) in bulk gas
C_S: concentration of reactant in surface gas
k: reaction rate coefficient
v: growth rate
N: atomic density, N_{si}=5x10^{22} atoms/cm^3
ΔH: activation energy

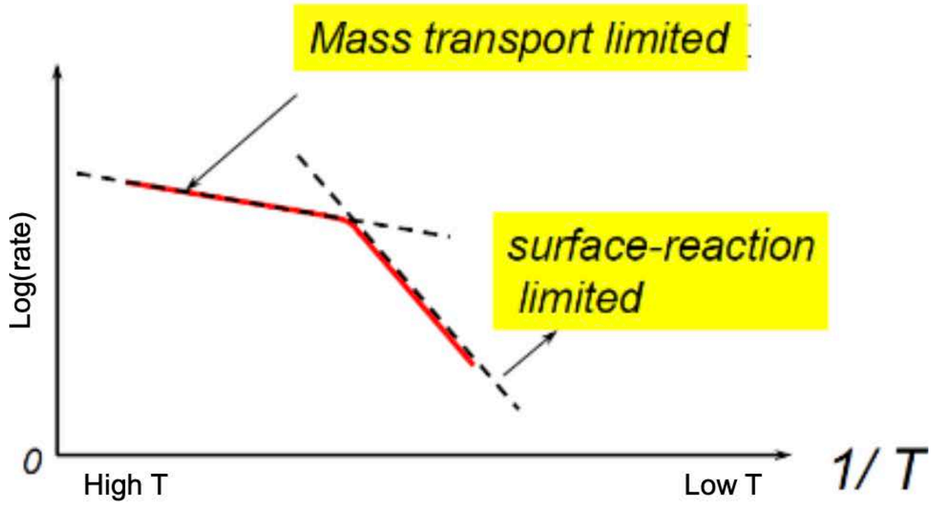
Chemical Vapor Deposition: Rate (Diffusion vs Reaction)

Diffusion Limited

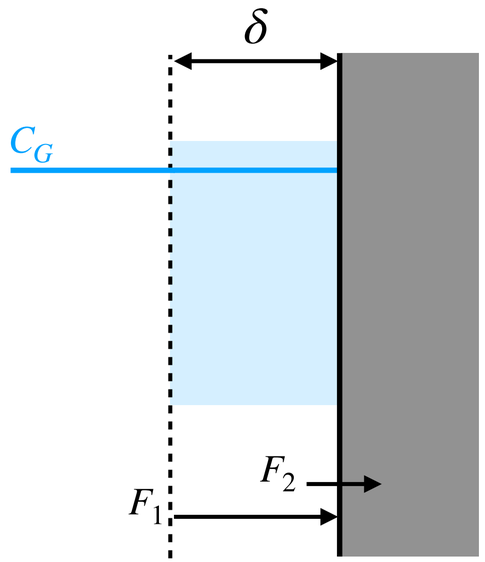


$$k >> h_G$$

$$v = \frac{h_G C_G}{N} \propto T^{\frac{3}{2}}$$



Reaction Limited



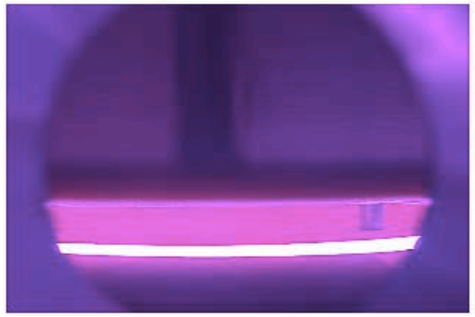
$$k << h_G$$

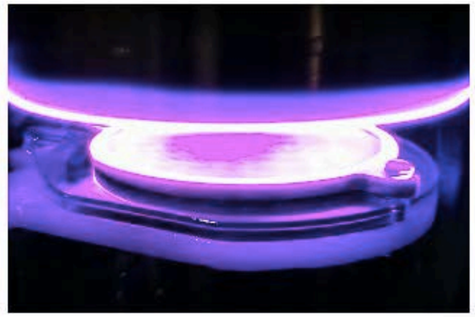
$$v = \frac{kC_G}{N} \propto e^{\frac{-\Delta H}{kT}}$$

Chemical Vapor Deposition: Plasma

allows for increase in Rate without increasing temperature

- non-thermal plasma: electron temperature high while the rest of the gas is at a lower temperature
- no damage to the existing structure





Chemical Vapor Deposition

Process Parameters

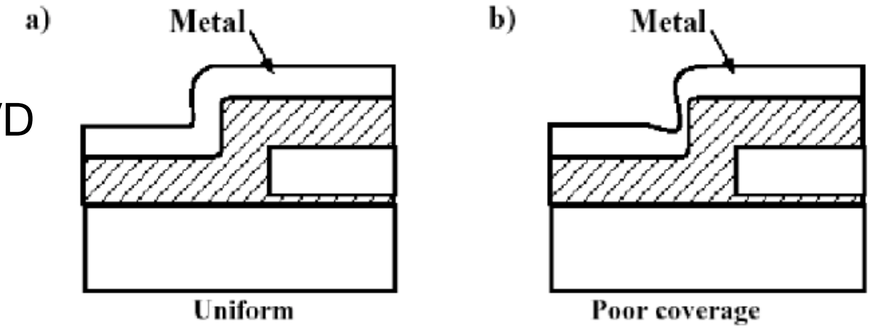
- temperature
- total pressure
- partial pressure of reactants
- flow rate of reactants and carrier gases
- time

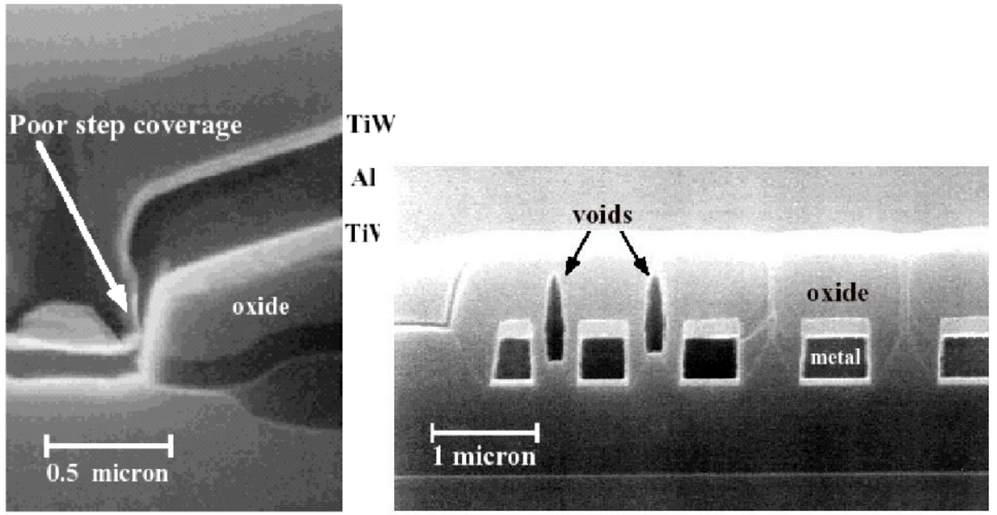
Control Parameters

- film thickness (~1-1000 nm and getting thinner - atomic layers)
- film deposition rate
  - poly silicon: ~hundreds nm/min
  - silicon dioxide: 10-100 nm/min
  - aluminum: 10s of nm/min
- film uniformity and quality

Quality

- better step coverage than PVD
- better for high aspect ratios
- void issues due to inconsistency/directionality

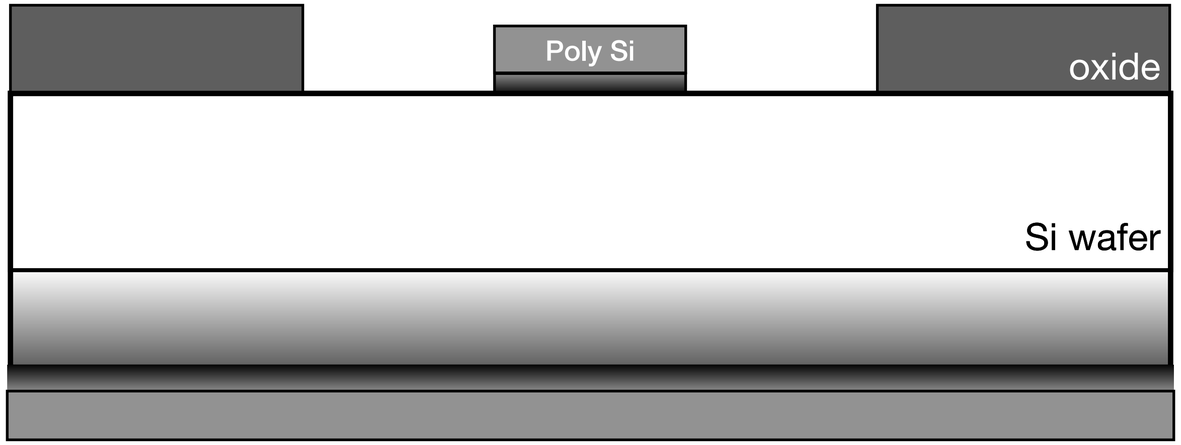




Process Flow Example: Pattern Poly Si

Pattern Poly Si

- deposit photoresist and develop
- dry etch poly Si
- remove photoresist



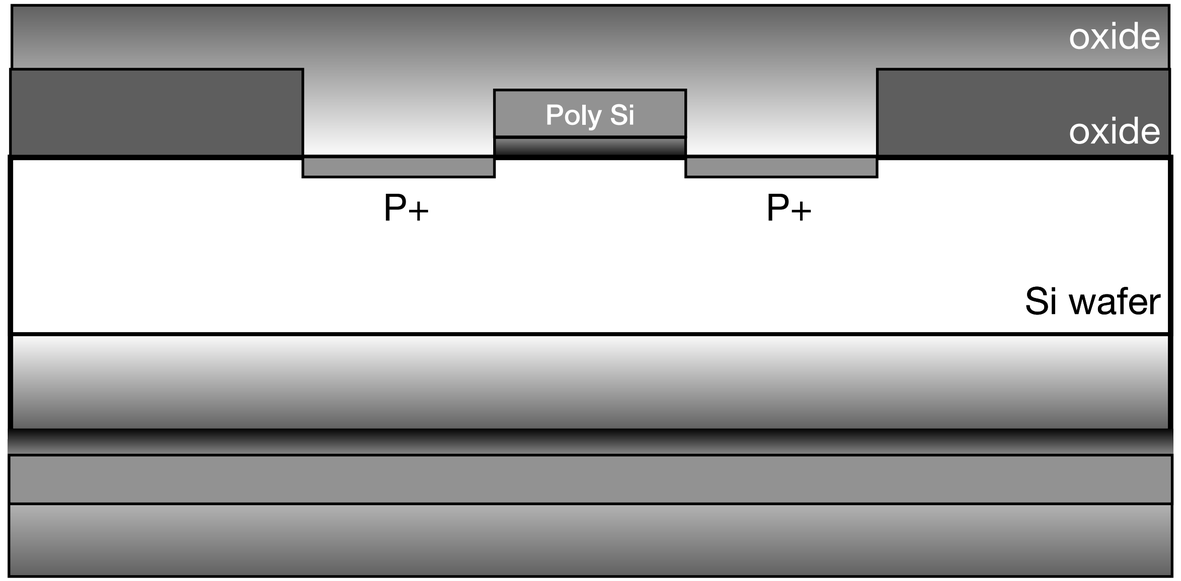
Process Flow Example: P+ Ion Implantation

Poly Si acts as a mask

P+ Ion Implantation

- Source/Drain P+ diffusion (tune electrical properties)

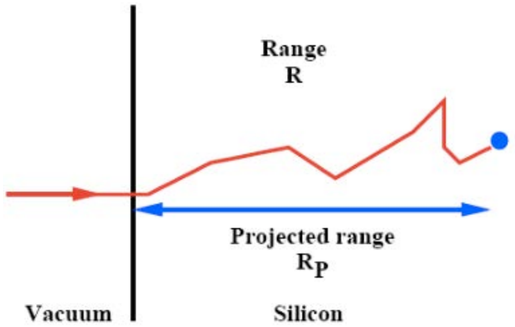
Reoxidation: fill in gaps and protect with a “roof”

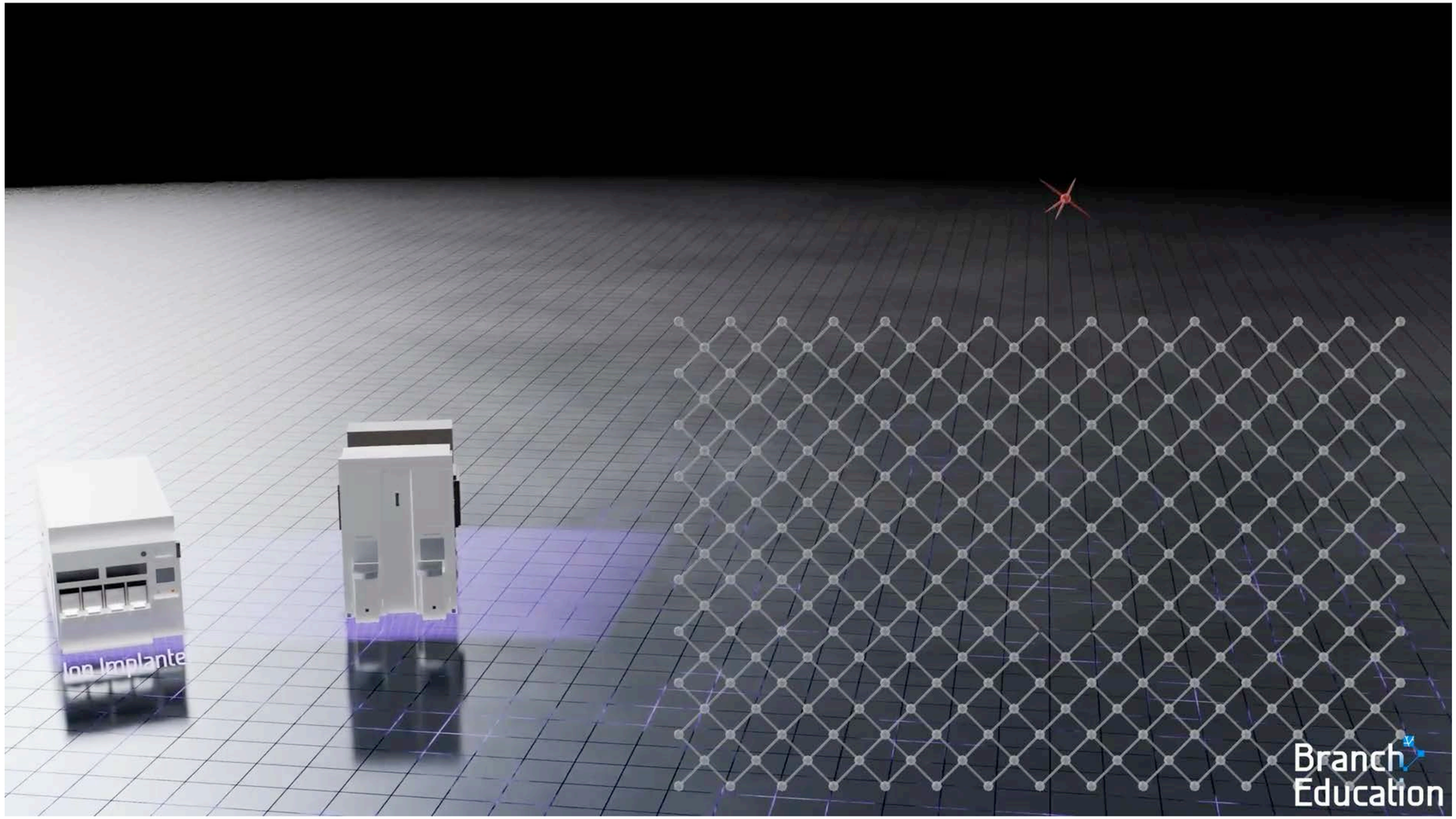


Ion Implantation

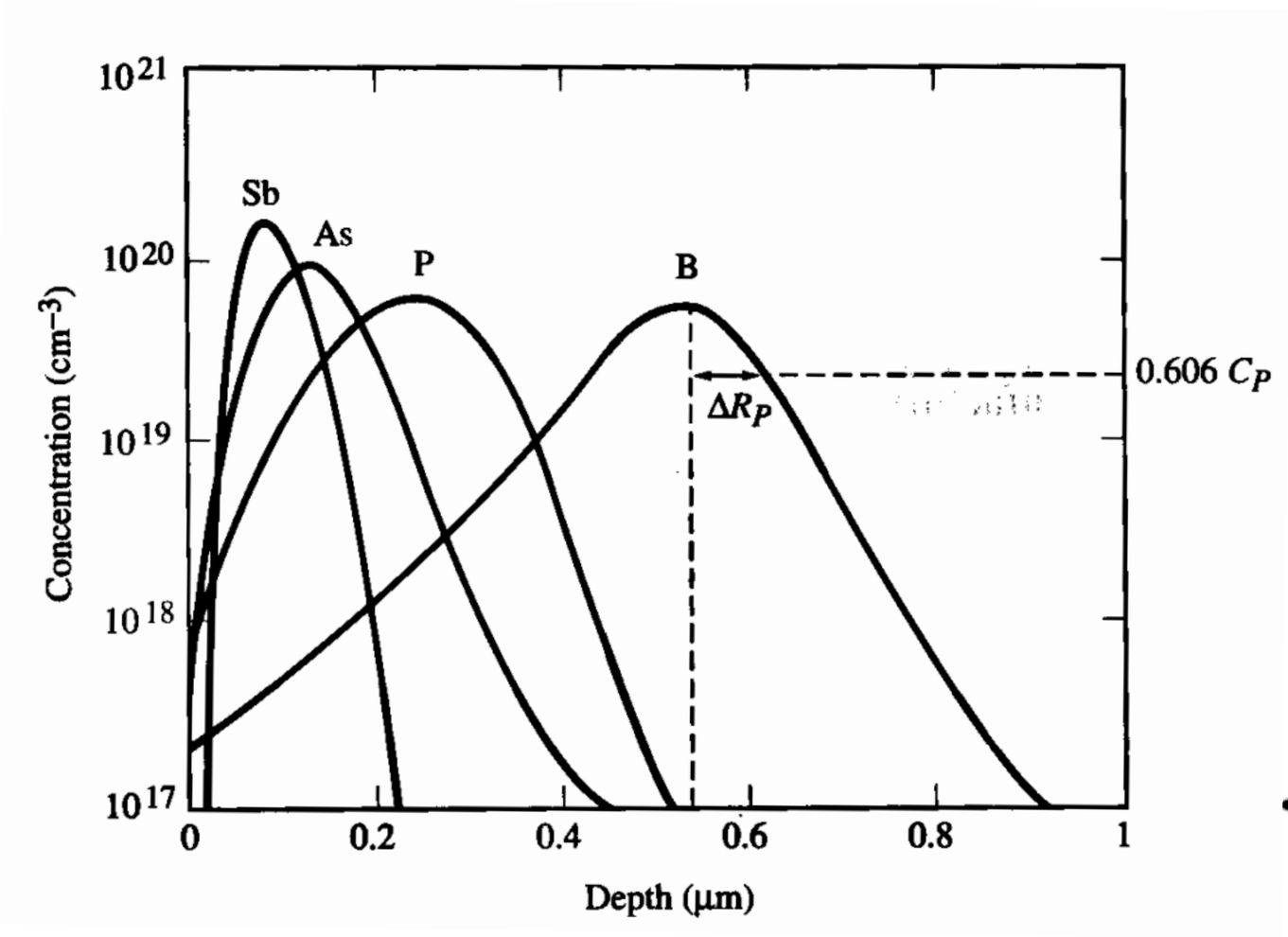
Random process: like shooting a gun of ions at a wall (silicon matrix)

- high energy (1-1000keV) ions bombard the substrate and lose energy through nuclear collisions and electronic drag forces



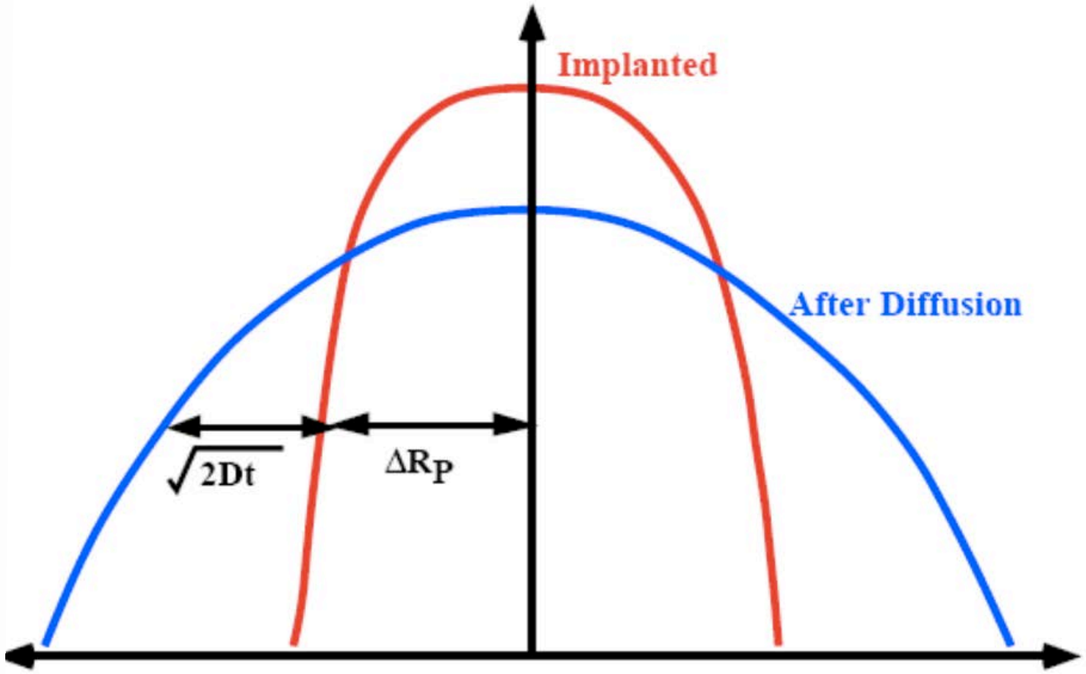


Ion Implantation



Normal Distributions!

- concentration vs depth into the silicon substrate
- standard deviation: called “straggle”



Ion Implantation

$$C(x) = C_P e^{-\frac{(x-R_P)^2}{2\Delta R_P^2}}$$ before annealing

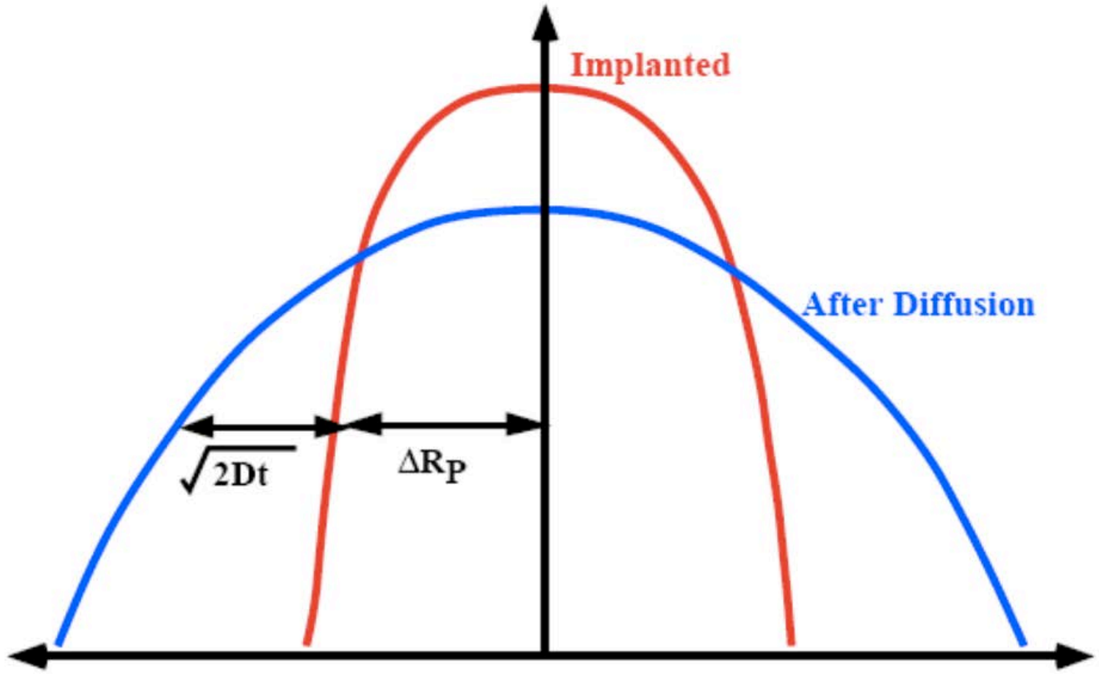
$$Q = \int_{-\infty}^{\infty} C(x)dx \rightarrow \sqrt{2\pi}\Delta R_P C_P$$

$$C(x,t) = \frac{Q}{\sqrt{2\pi(\Delta R_P^2 + 2Dt)}} e^{-\frac{(x-R_P)^2}{2(\Delta R_P^2 + 2Dt)}}$$ after annealing

C: concentration of ions
Q: ion dose
C_p: peak concentration
R_p: average projected range
ΔR_p: standard deviation or straggle
D: diffusion coefficient
t: annealing time

Normal Distributions!

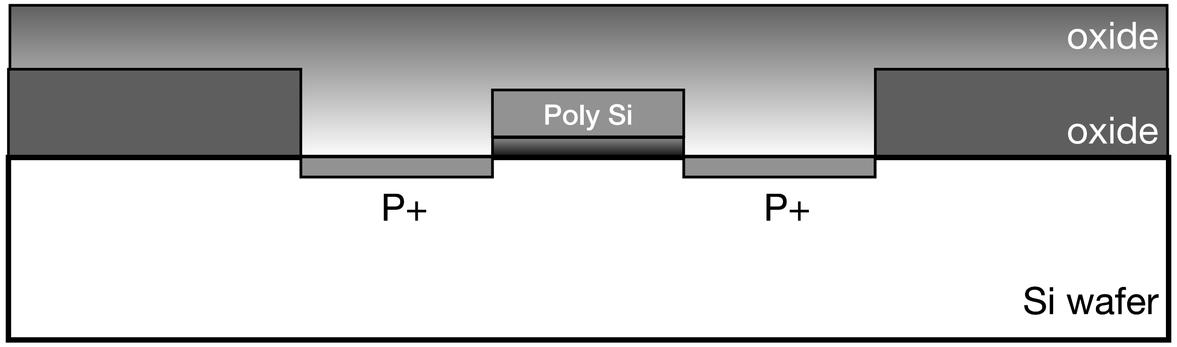
- concentration vs depth into the silicon substrate
- standard deviation: called “straggle”



Process Flow Example: Back Cleanup

Remove Oxide and Poly Si from back

- Oxide: BOE (Buffered Oxide Etch)
- Poly Si: Plasma etch

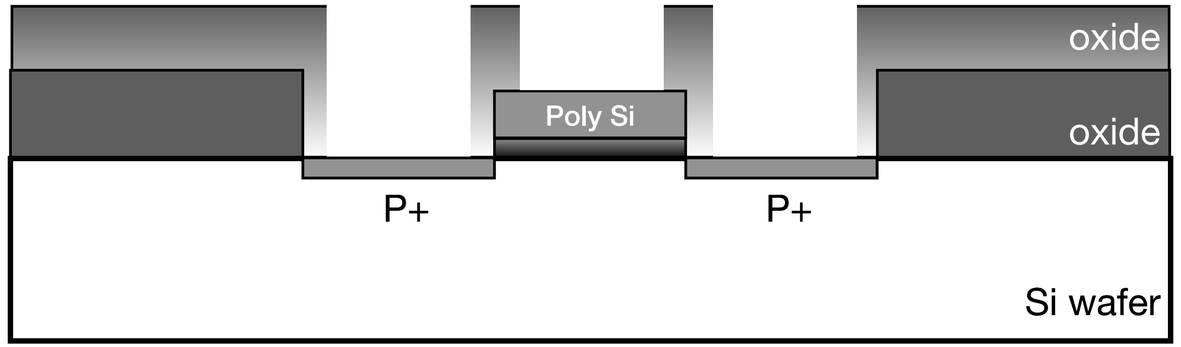


Process Flow Example: Pattern Al Interconnects

Planarization

Apply photoresist, expose, develop

Oxide etching



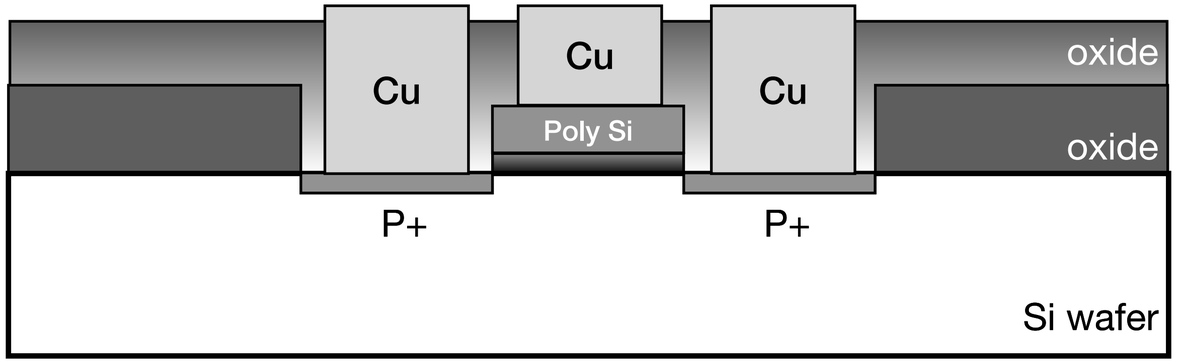
Process Flow Example: Al Metallization

Hydrofluoric Acid dip to strip oxide layer

- add copper layer

Done! Until you add more layers…

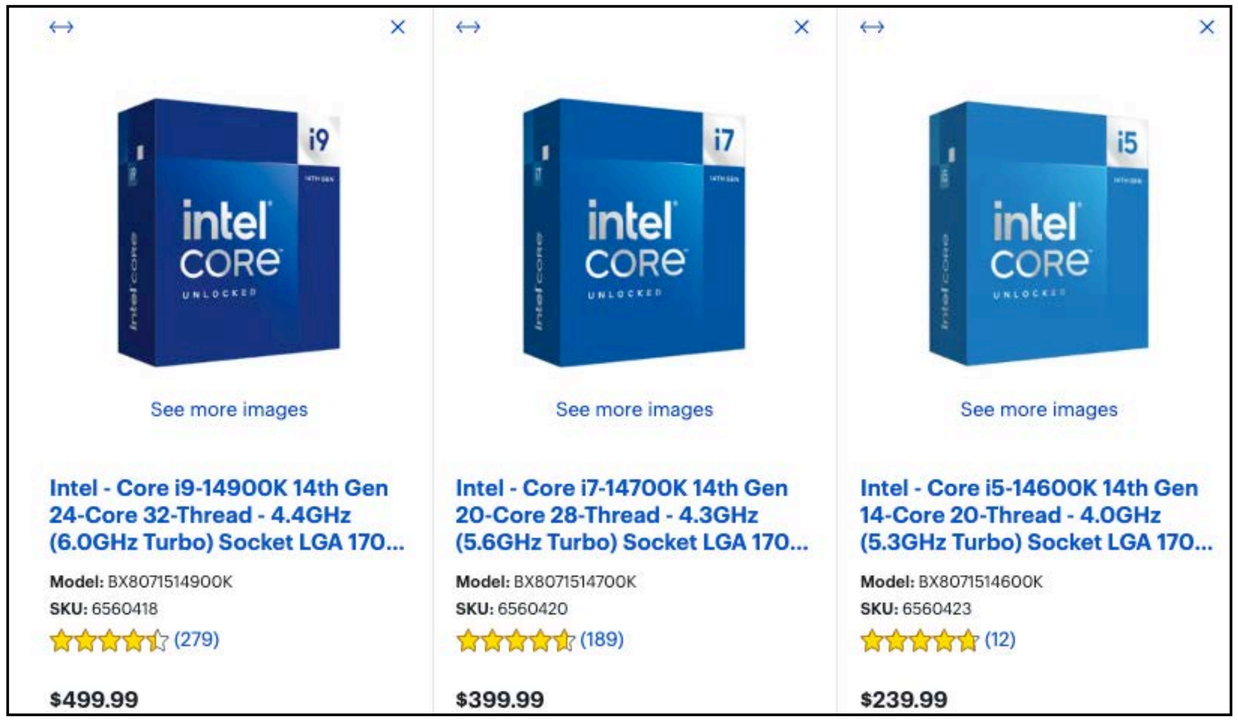
- treat these processes like a “tool kit”
- library of processes to use to make different devices



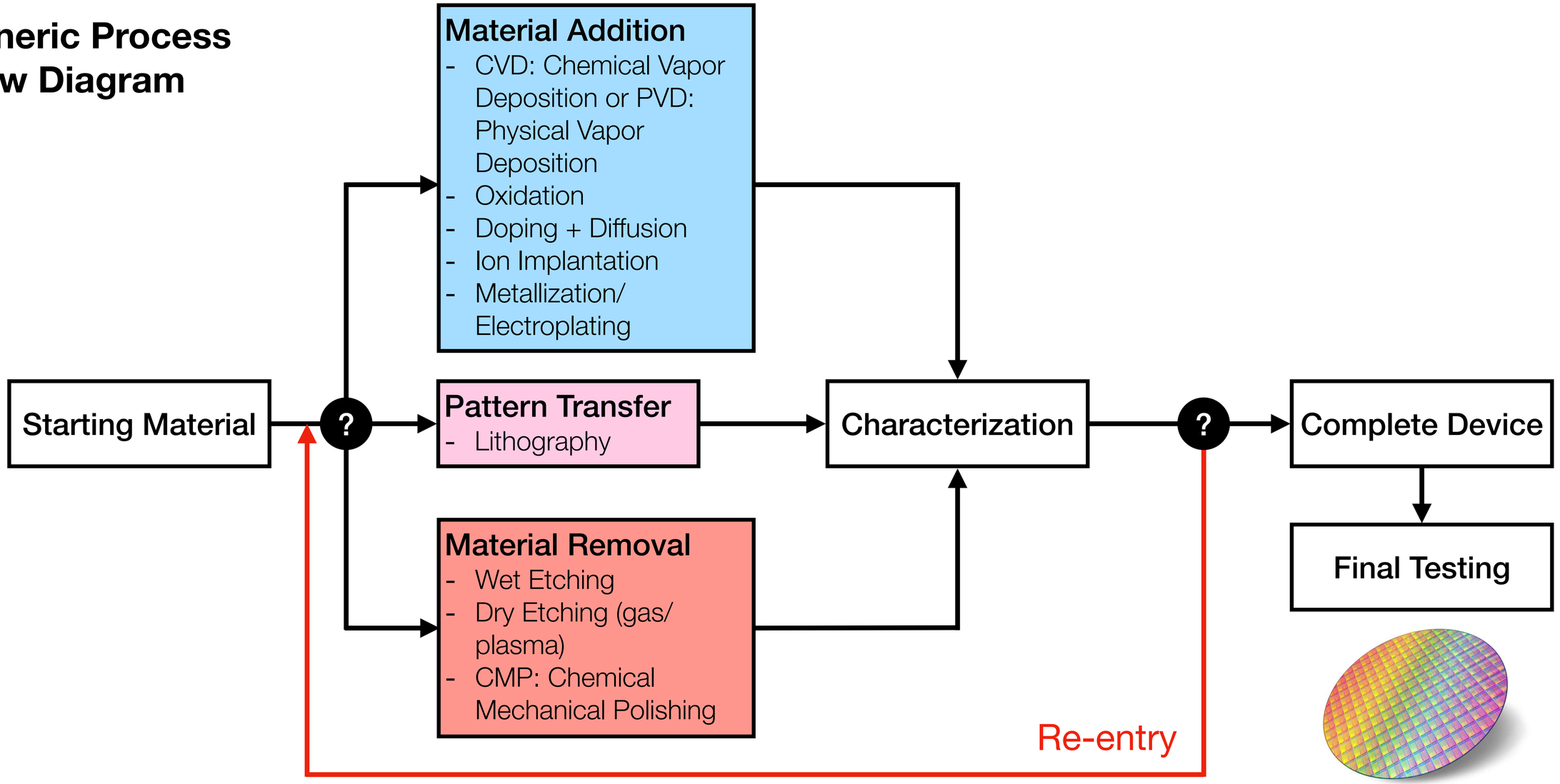
Manufacturing Attributes

Same stuff, different lingo

- production rate → throughput
  - 300,000 cars/year vs 60 wafers/hour
- yield: takes the until you are at production levels
  - don’t throw away lower performing chips
- cost of ownership: how much is costs to produce a chip or feature

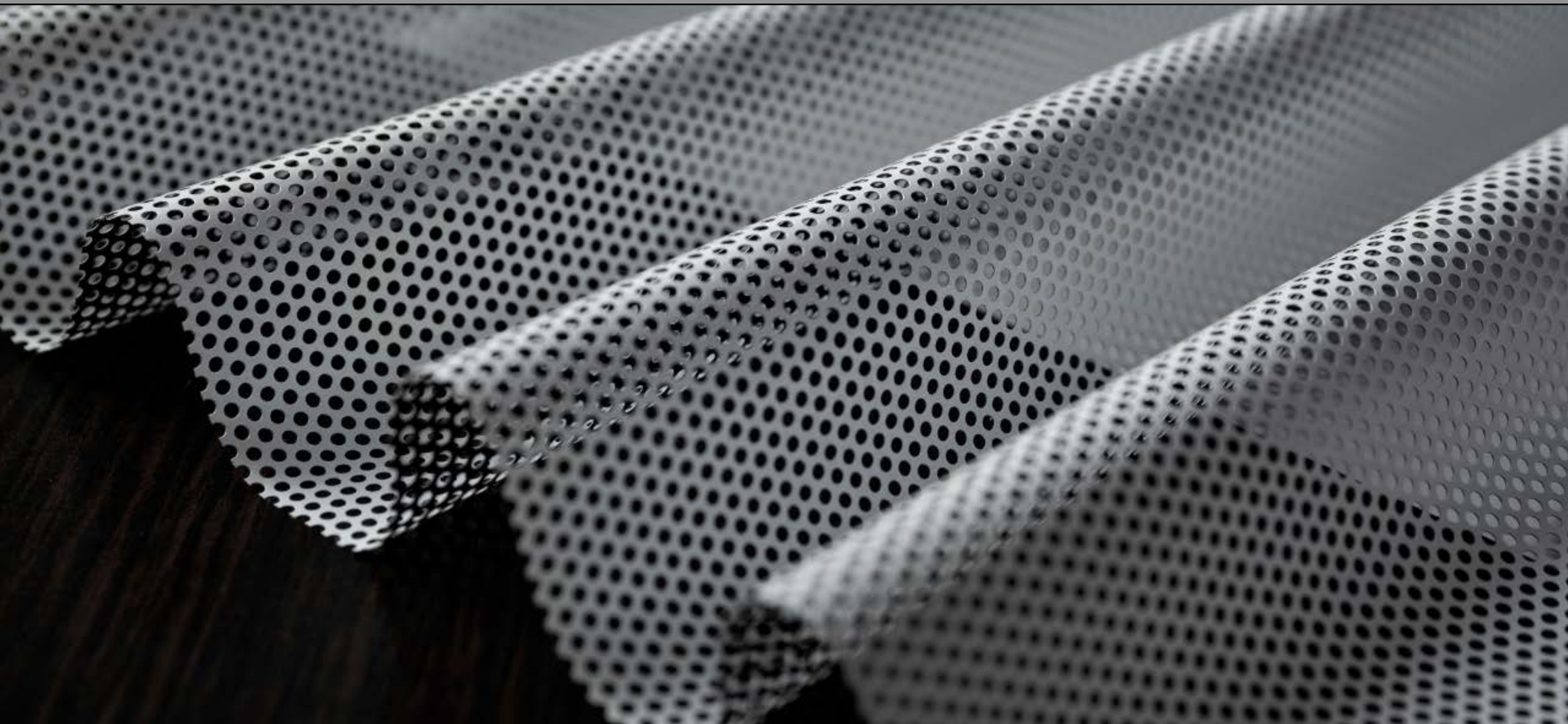


Generic Process Flow Diagram



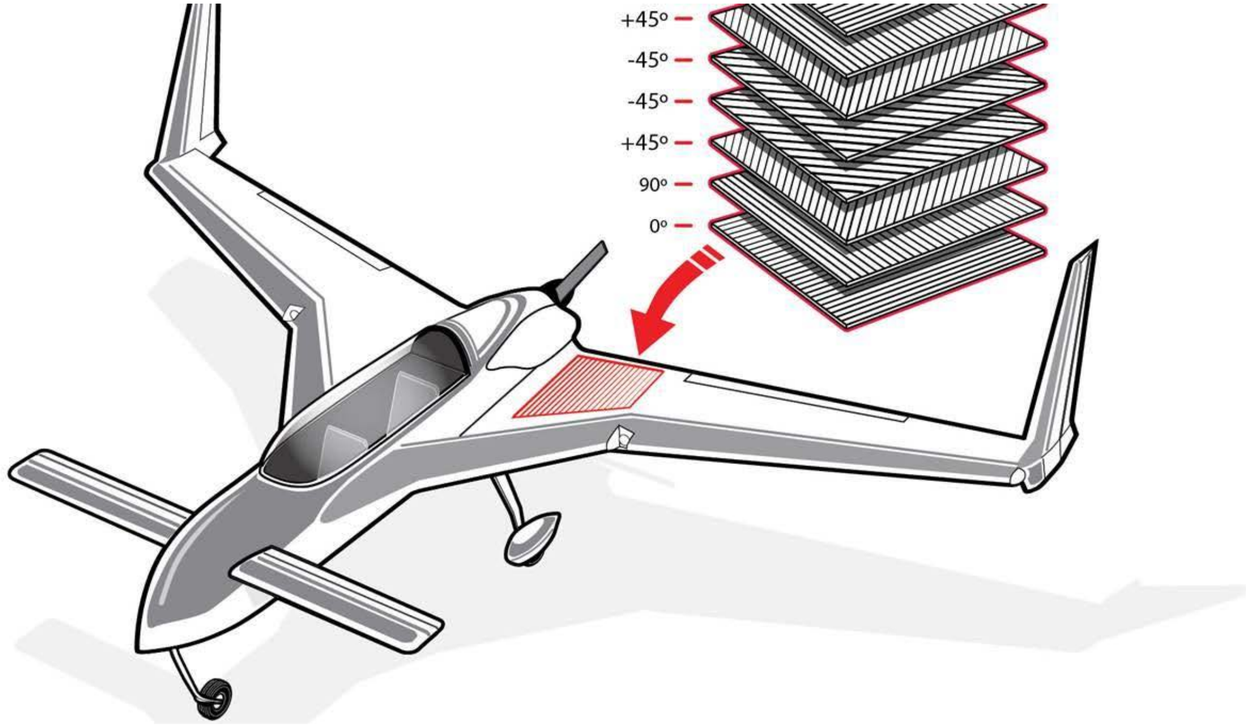
Layered Manufacturing

Polymer Matrix Composites



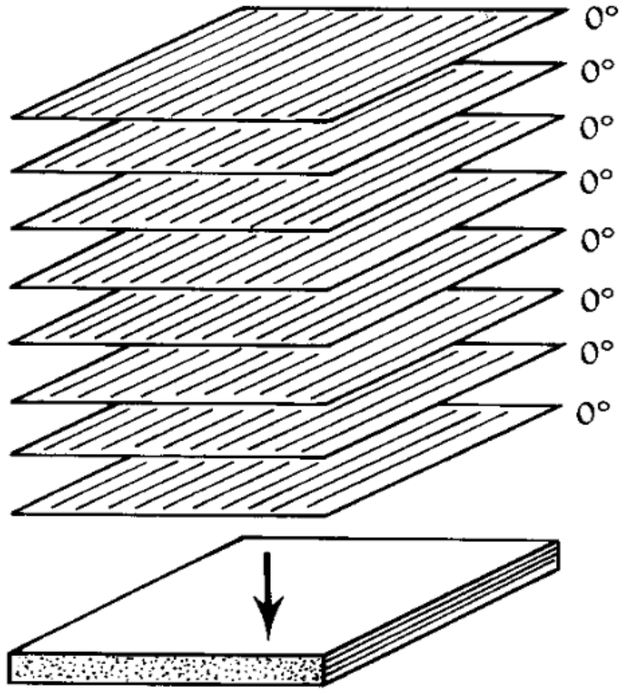
Polymer Matrix Composites

Sports Technology

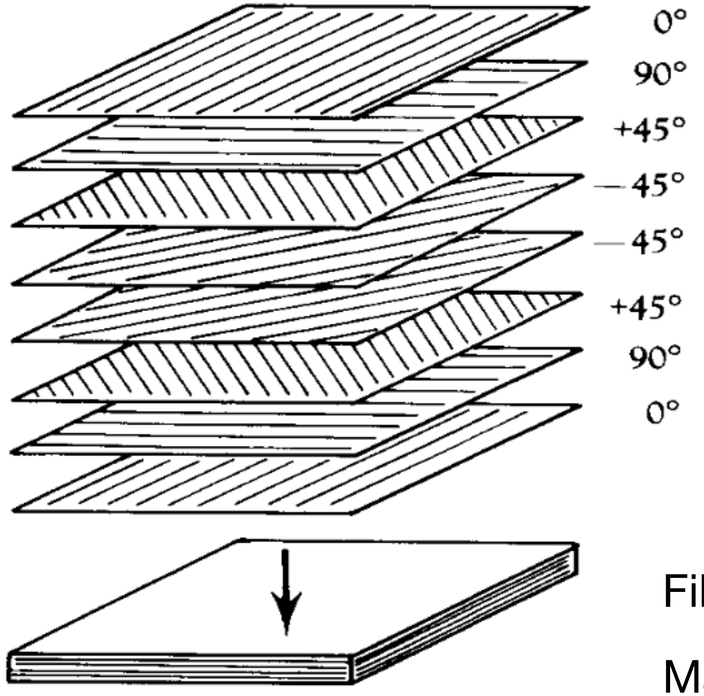


Aerospace

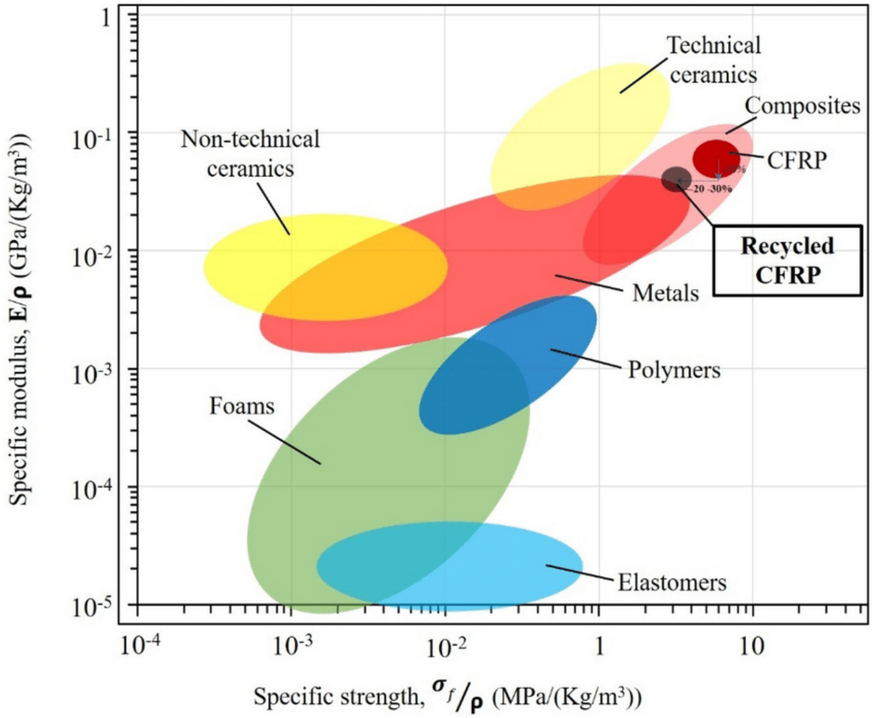
FRP (Fiber Reinforced Plastic) Composites



Anisotropic



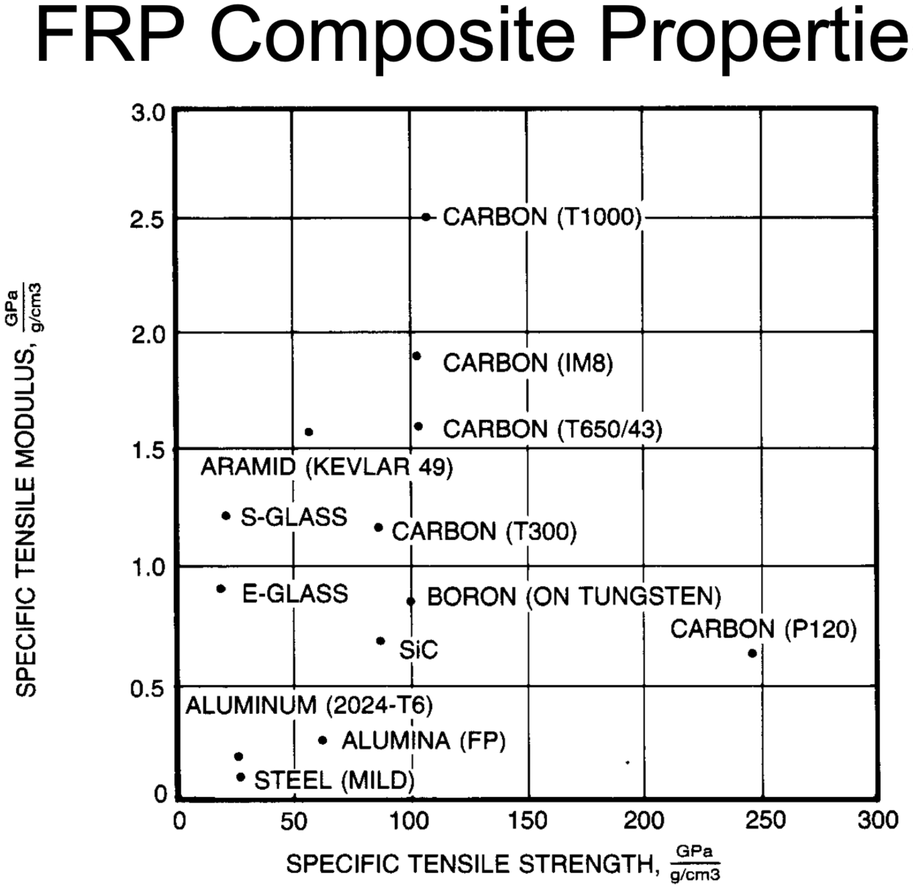
Quasi-isotropic



Fibers: glass, carbon, graphite, boron, kevlar

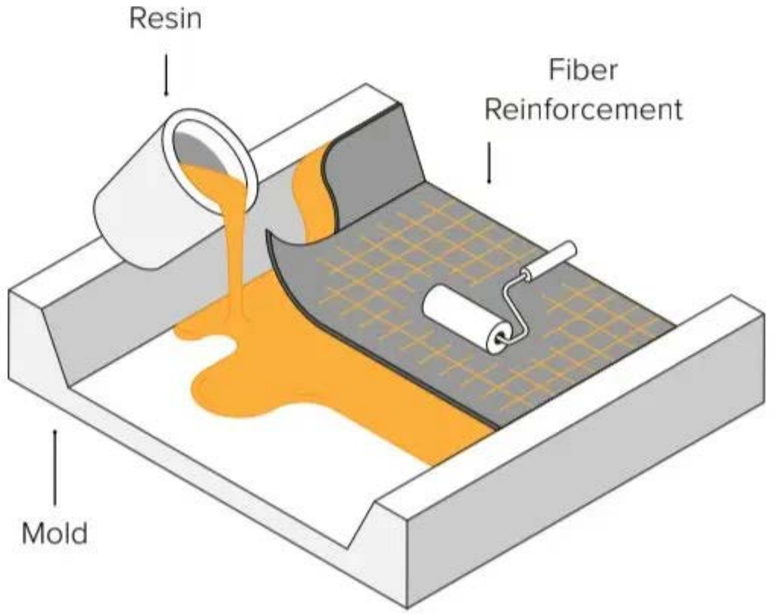
Matrix: thermosetting resins, thermoplastics

FRP (Fiber Reinforced Plastic) Composites

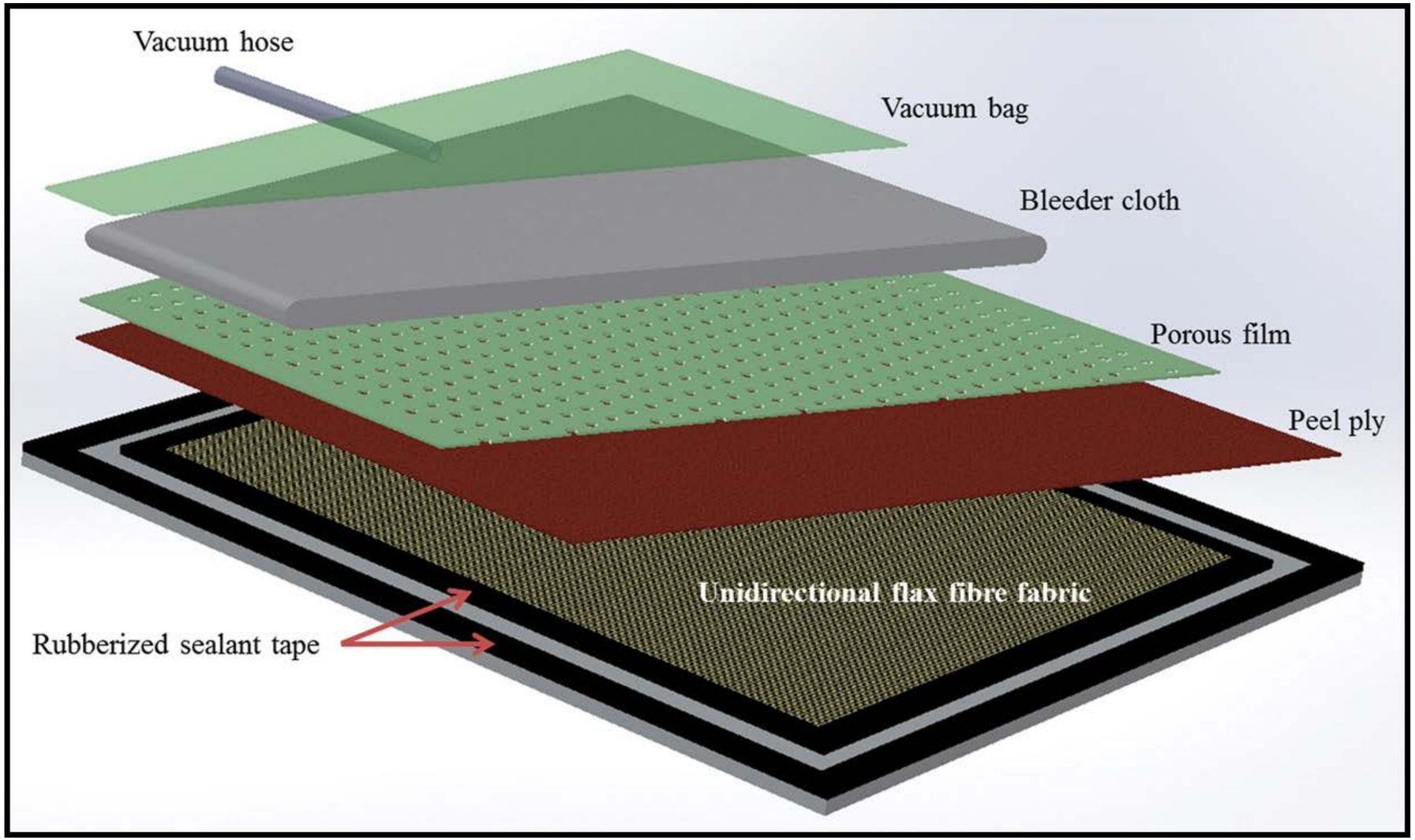


Comparison: steel, aluminum and composites (65% fiber)

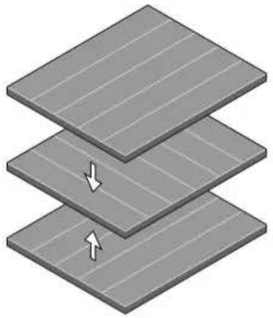
Hand/Wet Lay Up



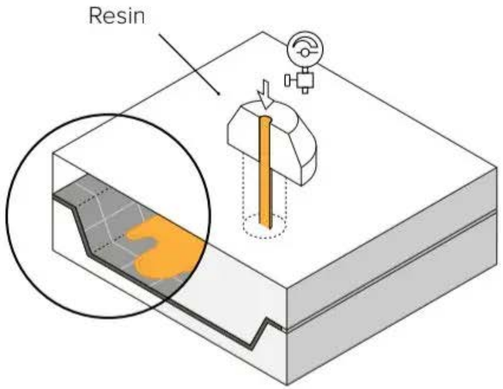
Vacuum Bag Molding



Resin Transfer Molding



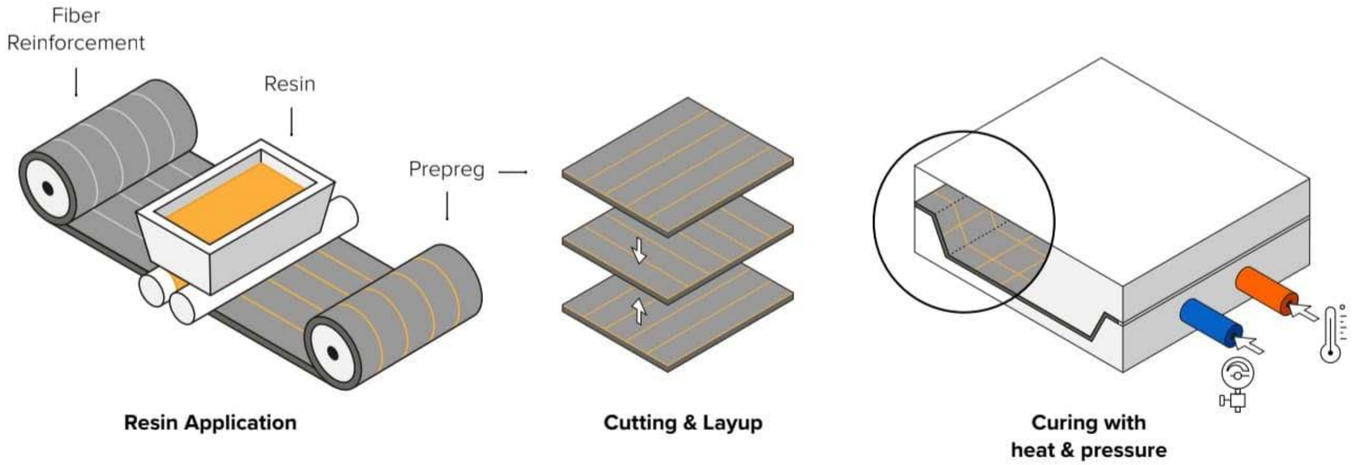
Cutting & Layup



Resin Injection

Pre-Impregnated Sheet Manufacturing

PREPREG PRODUCTION PROCESS



Autoclave Curing

pressure + temperature = $

Layered Manufacturing

Polymer Matrix Composites

Advantages/Disadvantages

compressive vs tensile strength

ability to repair

cost

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